Chapter 4

Electronic characterisation of $CuGaSe_2$ solar cells

In the previous chapter the structural features of $CuGaSe_2$ (CGSe) films and related devices were analysed. It was found that the absorber film quality shows a remarkable dependence on the deposition conditions, and thus it is of major interest to optimise the CGSe absorber growth process in order to improve the PV yield obtainable from these films in final devices. The most convenient way to evaluate the effects of different absorber deposition recipes is to compare directly the operation of solar cells processed in identical way from different absorber films. This procedure permits evaluating the influence of the different growth approaches on the electronic processes involved in the device performance, and constitutes the core of the present chapter. Therefore, we move now to the electronic performance and characterisation of complete devices, with particular attention to two main aspects:

- the realisation of a comparative study of device performance, assessing the different deposition approaches to an improved absorber film quality discussed in Chapter 3, and
- to establish the role of interfacial issues related to the electronic transport mechanisms governing the device performance.

Interfaces are a key element of any heterojunction-based device, as already mentioned in Chapter 2. Particularly, thin-film solar cells are characterised by the abundance of surfaces and interfaces in cross-sectional dimensions not larger than a few microns. In the present case, and excluding those interfaces related to grain boundaries, a number of layers (including glass, Mo, $MoSe_2$, CGSe, CdS, i:ZnO, Ga:ZnO, and Ni-Al front contacts) build up seven interfaces between them. The importance and direct impact of each of these interfaces on the operation of the final device is very different[j], and two of them will critically control the electronic transport in the solar cell, namely those involving the CGSe absorber layer. As the absorber layer is responsible of generating the charge carriers from the light, the electronic transport does principally consist of the extraction of those carriers from the absorber to the front and rear electrodes before they recombine back in the film bulk, as explained in Chapter 1. The success of this stage will be thus limited, firstly by the absorber bulk quality, and secondly by the electronic quality of the absorber related interfaces. Once the charge separation has taken place at the p-n junction, recombination currents will dominate the transport, as reviewed in Chapter 2, relaxing the impact of other interfaces in the device operation.

We start this chapter with the study of the CGSe/CdS interface formation on state-of-the-art two-stage CGSe devices based on chemical vapour deposition (CVD). This

[j] Fortunately, not *all* these interfaces are critical; otherwise, the operation of such devices would have to be considered extraordinary.

interface is the actual p-n junction driving the device operation, despite of the fact that most of the energy band bending built up at the heterojunction results from the subsequent deposition of the window n^+-ZnO material, as it will be shown in Section 4.1. However, the band offsets at the CGSe/CdS interface, as well as the interface quality regarding the presence of surface states, will determine the extent of losses in the open circuit voltage to be expected and the importance of interface recombination of minority carriers at the junction during the device operation. The study of the electronic transport in CGSe devices constitutes the second part of the chapter (Sections 4.2 and 4.3), where the quality of the main CGSe/CdS junction will be assessed. Furthermore, evidences of the role the $MoSe_2$ interfacial layer at the rear contact plays in the device operation will be presented, concluding that certain modifications in the energy band diagram are mandatory in order to account for the experimental observations.

4.1 Study of the CGSe/CdS interface

The CGSe/CdS interface constitutes the p-n heterojunction. As the critical component, its properties and quality determine the dominant electronic transport mechanisms governing the device performance. These are in turn the result of the energy band alignment between the materials building up the junction and of the impact of interfacial electronic states resulting from the mismatch of crystal lattices of two dissimilar materials.

The energy band line-up characterises the properties of semiconductor heterojunctions. When bringing together two dissimilar materials with different properties, including different energy band gaps, a certain equilibrium situation results, characterised by the constancy of the Fermi level across the entire device. Band offsets will appear at the metallurgical junction, resulting in convenient or inconvenient features for the electronic transport across the junction. A review of different possibilities of band line ups in semiconductor heterojunctions can be found in Ref. [178]. The knowledge of the band offsets is thus important, as it allows to asses the p-n junction operation. Subsequent predictions on modified line-ups (e.g. after energy band gap engineering or from the substitution of the buffer material) can in turn be deduced from band alignment considerations[179].

The starting point for the theoretical analysis of semiconductor heterojunctions is Anderson's model[180], which assumes an abrupt junction and neglects contributions from interface dipoles and surface states. In his classical work, Anderson reported on the fabrication of isotype (n-n, p-p) and anisotype (p-n) junctions based on Ge/GaAs heterojunctions, and introduced the basics of the heterojunction theory for the prediction of their related electronic properties. The key element of the theory is the statement of a common reference level to which all energy levels of each compound are referred to. In Anderson's model, this is the vacuum level, which by definition is continuous through the whole cross-section of the device. The fundamental parameters that determine the band line up between the semiconductors building up the heterojunction are then their electron affinities χ_1 and χ_2 (defined as the energy difference between the bottom of the conduction band and the vacuum level) and their energy band gaps E_{g1} and E_{g2}. When both parameters are known for each pair of semiconductors, the resulting band line up of the given heterojunction can in principle be inferred from simple calculations:

- The conduction band offset will be determined by the difference of electron affinity values on either side of the heterojunction:

$$\Delta E_{CB} = \chi_1 - \chi_2 \quad \text{Eq. 116}$$

- The valence band offset will in turn be determined by:

$$\Delta E_{VB} = (\chi_1 + E_{g1}) - (\chi_2 + E_{g2}) \quad \text{Eq. 117}$$

An interesting aspect of this approach, known as the *electron affinity rule*, is that the band offsets so derived are independent of the doping concentrations (as long as the electron affinity and the band gap do not depend on the doping, i.e. in non-degenerated materials), allowing to separate the band offset problem from that of the energy band bending on either side of the junction, the latter in turn being determined by the doping (or equivalently the work function) and the corresponding voltage drop, as discussed in Chapter 1. Therefore, once the band offsets at the junction have been estimated from the electron affinity rule, Eq. 12 can be used to completely solve the problem of the band alignment and to depict a comprehensive band diagram of the device under equilibrium conditions.

In practice, this simple picture fails in fully describing the heterojunction properties. Firstly, it assumes an abrupt junction formation, the actual realisation of which will depend on the surface reactivity and element intermixing of both junction partners. Even if such ideal plane-confined type of junction can be provided (and this can be experimentally done e.g. by epitaxial growth and by chemical bath deposition, CBD, as shown below), the intimate contact area will be critically affected by the lattice mismatch resulting from two dissimilar crystal structures (at least with dissimilar lattice constants), inducing crystal defects and strain. The immediate consequence of these issues is the appearance of electronic states confined at the interface, which are known to be either effective recombination or trapping centres of charge carriers. Furthermore, electric dipoles may appear even at perfectly terminated surfaces, e.g. in compound semiconductors such as CGSe, if the surface on which the junction will form has a polar nature (i.e. a different number of cations and anions per surface unit cell). The net charge accumulation at surface states and the effect of electrostatic dipoles alter the simple potential distribution that would be expected from the simple diffusion model of the p-n junction. Subsequent refinements to Anderson's theory have been proposed, a critical review of which can be found in Ref. [181].

Nevertheless, basing on practical considerations, the simple model from Anderson will be adopted for the analysis of the CGSe/CdS interface under study (and additionally to the rear CGSe/$MoSe_2$ interface reviewed later). This decision is supported by the following considerations:

- TEM observations (see Figure 63) reveal a well define metallurgical junction, a basic requirement of the depletion region approximation leading to Eqs. 116 and 117, and the electron affinity rule that permits the estimation of the band offsets.
- The polycrystalline nature of the semiconductors forming the interface makes unaffordable even the simplest attempts to estimate the contributions of interface dipoles, defect densities and lattice mismatch for every single pair of crystallite surfaces coming in contact during the junction formation. The case is even more

complicate if one of the junction partners presents more than one crystalline phase, as it is the case of CdS deposited by CBD at 60°C (see below). Indeed, it could be argued that the polycrystallinity may act neutralising some of these effects (in particular the contribution of surface dipoles), provided a random distribution of crystallite orientations (i.e. approximately equal number of metal- and chalcogen-terminated facets in the case of CGSe) at the junction plane.

- Anderson's model is invariably used to predict energy band diagrams of semiconductor heterojunctions, and a reasonable agreement between the theory and the experiment is normally found regarding the band offsets (not necessarily in the expected transport properties)[181]. Microscopic factors which determine the local charge distribution are estimated to contribute by not more than 0.1-0.2 eV to the band offsets, according to Ref. [182], thus lying in the range of experimental resolution by electron photoemission in the determination of the band offsets. A substantially different case is the formation of Schottky junctions between metals and semiconductors, where the resulting potential barrier heights are experimentally far from following the theoretical predictions of the equivalent Anderson's model (see for instance Ref. [183]).

Based on these considerations, the approach followed in this Chapter for the study of the absorber heterojunctions will consist in the application of the electron affinity rule for the estimation of band offsets. The subsequent study of the electronic transport will determine the validity of the approach, yielding additionally quantitative information on the electrostatics (i.e. potential distributions, SCR width, role of interface states, etc.) of the junction.

The study of the heterojunction formation between CVD-grown CGSe absorber films and CBD-deposited CdS buffers was carried out by means of photoelectron spectroscopy measurements (XPS and UPS) on a series of samples from the same two-stage process, on which different buffer deposition times were processed. This technique is widely used for the estimation of the valence band offset at semiconductor heterojunctions. The fact that in the present case the covering species (CdS) possesses a larger band-gap than the substrate species (CGSe) prevents the application of the so-called *direct* method[182,184] of valence band offset estimation, based on UPS spectra on the evolution of the valence band (VB) edge as a function of coverage. The *indirect* method[185] must thus be applied in order to take into account the possible band bending induced by the coverage, whose reliability has been demonstrated in a number of studies on $CuGaSe_2$ [(186,187], $CuInS_2$ [(188,189] and $CuInSe_2$ [(190] samples. This method consists in the measurement of the valence band edge of substrate and adsorbate species, with respect to the reference position of core levels of each species. The valence band offset is given by:

$$\Delta E_V = BE_{CL}^{VBM}(CGSe) - BE_{CL}^{VBM}(CdS) - \Delta E_{CL} \qquad \text{Eq. 118}$$

where BE denote the core level to valence-band maximum binding energy difference of each compound and ΔE_{CL} represents the difference between core level binding energies of pairs of elements from each junction partner at low coverages, when the information depth of the emitted photoelectrons is sufficient to sample both substrate and adsorbate.

A batch of six CGSe samples were prepared in the CVD reactor following a standard two-stage process. The samples were transported in nitrogen atmosphere by means of a

transfer chamber to a glove box preparation chamber, connected to the photoemission set-up. The chemical bath was performed under nitrogen atmosphere following the recipe described in Section 1.3. CGSe samples were immersed in the chemical bath during different times, from 20 to 420 seconds (the latter being the standard deposition time providing a buffer layer to the solar cell), keeping a bare CGSe absorber as reference for the calculation of core level shifts due to band bending and/or chemical shifts.

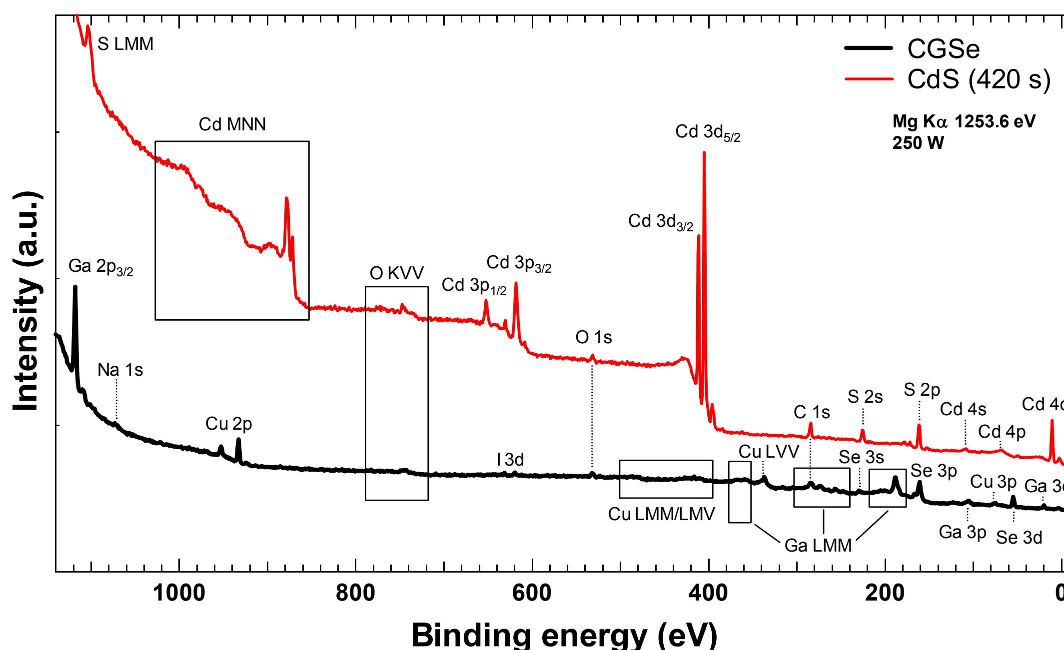

Figure 59. XPS overview spectra of reference samples (CGSe bare absorber and CdS buffer layer after 7 minutes of CBD processing). Mg K_α (1253.6 eV) was used as excitation source, with 20 eV pass energy.

Figure 59 shows XPS spectra of the two samples used as reference for the band offset calculations, the bare CGSe absorber and the fully processed buffer on it. The spectra were recorded in normal emission using Mg K_α radiation as excitation source, using 20 eV pass energy at the hemispherical electron analyser, operating under UHV conditions (base pressure $5\cdot10^{-10}$ mbar). The core level identification was carried out with the help of standard literature[191]. Both samples appear relatively clean, showing minor oxygen and carbon peaks, attributed to adsorbates originated from the solutions of the chemical bath. Additionally, traces of iodine and sodium appear on the CGSe bare surface (the I 3d doublet visible at 619 eV, the Na 1s singlet at 1072 eV). Regarding the presence of iodine, which is used as transport agent in the CVD process, similar results have been observed by Fischer[79] and Meeder[38] on CVD-grown CGSe samples, concluding that the halogen is located on the CGSe surface, with no detectable incorporation in the sample bulk, as inferred from XPS measurements after Ar^+ sputter cleaning, and from compositional depth profiles by Elastic Recoil Detection Analysis (ERDA). In the present study, it is inferred that iodine forms a soluble species on the CGSe surface, as the corresponding iodine photoemission signal disappeared after 20 seconds processing in the CBD, while the information depth of the emitted photoelectrons still allows to sample the underlying CGSe film. Similar conclusions are deduced for the sodium, known to diffuse from the sodium-containing glass substrate and to segregate at

surfaces of chalcopyrite compounds, and also found in the study of Meeder[38] on CVD-grown CGSe. Contrarily to the case of iodine, an upper limit of 0.06 at.% could be inferred from ERDA measurements regarding the sodium concentration in the CGSe bulk[50], which is reported to increase the conductivity of the films[1]. The formation of NaI accounting for the observed features (and in particular for the solubility in aqueous solution of the compound), implicitly excluded in the study from Meeder *et al.*[50], is considered unlikely based on the observed binding energies[191]. Alternatively, it was proposed in Ref. [50] that free iodine may form Ga_xI_y during the cooling stage of the CVD growth, whereas a fraction of the sodium present at the surface can be incorporated into the chalcopyrite matrix at the expense of Cu depletion at the surface. Studies of Niles and co-workers[192] on the interaction of Na with $Cu(In,Ga)Se_2$ samples pointed to the formation of Na-Se segregations at the chalcopyrite surface, supporting a relevant role attributed to Na-Se-O compounds in the passivation of surface states, once the sample has been exposed to air[193,194]. Additionally, explanations relying on interfacial Na, such inducing an altered valence band offset or a different growth morphology for the CdS, that may account for the beneficial effect of Na incorporation into the chalcopyrite on the PV performance, were explicitly excluded in the paper from Niles *et al.*[192] basing on the experimental observation that water removes the surface Na, e.g. during the CBD processing. The chemical bath thus provides an effective surface cleaning and indeed, a soft etching of the chalcopyrite surface cannot be excluded.

Figure 60 shows a series of XPS spectra of the valence band region of the set of samples after each buffer deposition step. Ga 3d core levels are also visible in the substrate reference sample (bottom, 0 s). With increasing deposition time the substrate coverage proceeds on, and CGSe emissions are gradually replaced by those characteristic from CdS. Ga 3d emissions are still visible after 40 s of buffer deposition (correspondingly 4.75 nm thickness, assuming a constant growth rate), together with the Cd 4d peak. The uppermost spectrum (420 s) corresponds to the complete buffer layer, with a nominal thickness of 50 nm, which serves as CdS reference, shown in the XPS overview spectrum of Figure 59. No evidence of additional chemical species is observed, excluding the formation of intermixing compounds, such as those discussed in Chapter 3 in the case of non-treated Cu-rich absorber films.

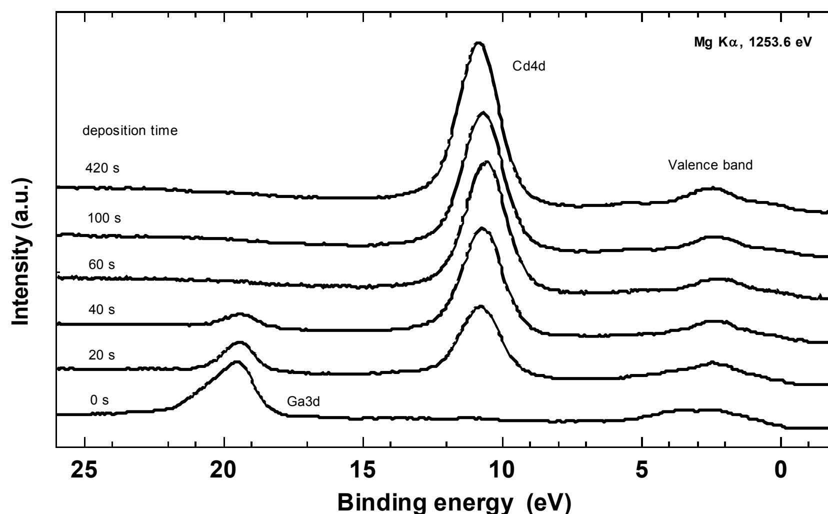

Figure 60. Photoelectron spectra of Ga 3d, Cd 4d and valence bands of CGSe in the course of CdS deposition.

A total band bending associated to the junction of up to 0.15±0.1 eV results from the buffer layer deposition, as inferred from the core level shifts recorded as a function of the coverage. These, and the relative peak intensities as a function of the buffer deposition time, are summarised in Figure 61. The decay of the Ga 3d absorber signal seems to follow an exponential law (linear in the semilogarithmic plot), which would be in agreement with a layer-by-layer coverage as a function of the deposition time. However, the limited number of experimental points limits the validity of the statement.

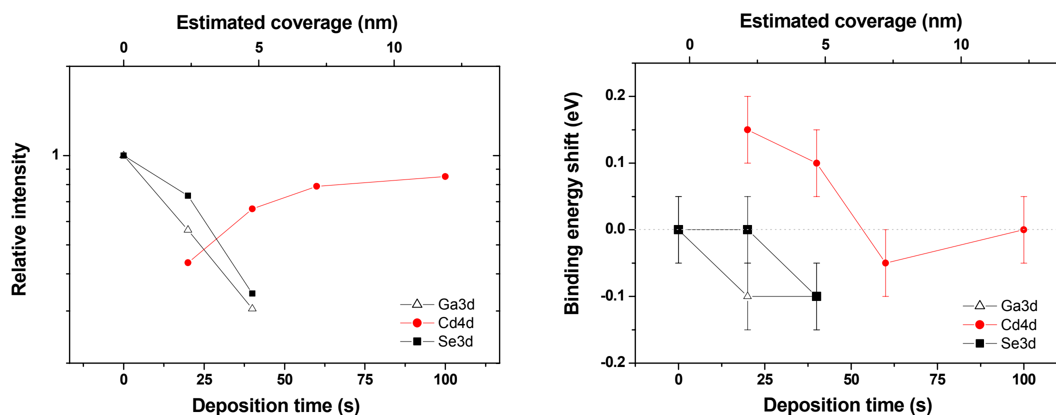

Figure 61. (Left) Relative intensity of core levels as a function of deposition time and estimated coverage thickness of the CdS buffer layer. **(Right)** Binding energy shifts of core levels as a function of deposition time and estimated coverage thickness of the CdS buffer layer.

In addition to the determination of reference core levels, the application of Eqs. 117 and 118 for the estimation of the valence band offset between the absorber and buffer layers requires the determination of the energy of the valence band edge of each compound with respect to the Fermi level. UPS was used for this purpose, by means of both He I and He II emissions. A gold foil, sputter-cleaned with Ar^+, served as reference for determining the Fermi level (zero in the abscisa). The energy difference between the valence band edge and the Fermi level was obtained from the linear extrapolation of the leading valence band edge on each sample over the background level, as shown in Figure 62, from which values of E_V-E_F=1.9 eV for CdS and E_V-E_F=0.8 eV for CGSe were inferred. The method provided a resolution of ±0.1 eV, as inferred from the sharpness of the gold Fermi-edge used as reference.

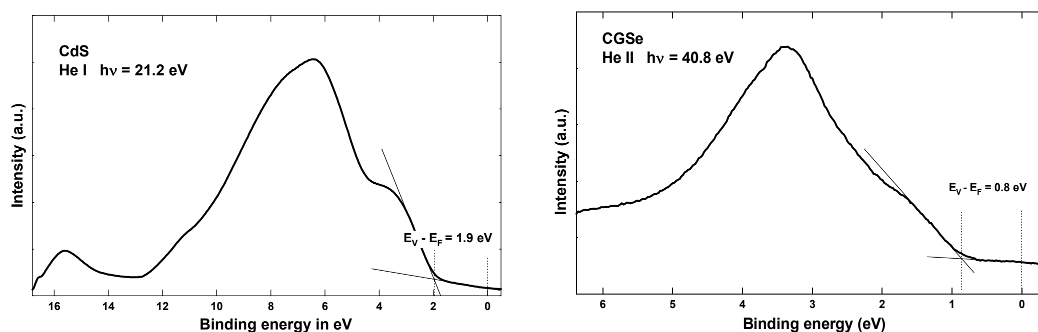

Figure 62. UPS spectra of CdS **(left)** and CGSe **(right)**, under He I and He II irradiations, respectively. Positions in energy scale of valence band edges are included referred to the Fermi level.

The values obtained in Figure 62 for the energy difference between the valence band and Fermi level are in good agreement with those found in the literature. Values of E_V-E_F = 0.8 eV have been reported by Schmidt[53] and Nadenau[186] for the top surface of Ga-rich CGSe samples, pointing to a highly compensated (nearly intrinsic) surface region. From simple calculations following Eq. 3, free carrier concentrations below 10^6 cm^{-3} would be obtained at room temperature from such value of E_V-E_F, which are far too low to account for the observed values of the film resistivity[38] and are in severe disagreement with estimations based on Hall measurements[66]. It is concluded that the position of the Fermi level with respect to the valence band edge at the film surface is substantially different from that expected in the film bulk. Whether this is the result of charge carrier depletion due to the appearance of donor-like surface states, or it should be related to a different phase of disordered nature, as discussed in Chapter 1, remains unclear. Strong evidences have been found of deviations from the bulk composition at the surface of chalcopyrite compounds[49]. Combined photoemission and inverse photoemission studies on CVD-grown CGSe samples of various compositions have been performed by Meeder *et al.*[50] reporting on enlarged band gaps at the surface (up to 2.0 eV in the case of two-stage samples), compared to bulk band gaps obtained by optical measurements. Similar band gap enlargements have been found in $CuInSe_2$, attributed to Cu-depletion at the near surface region[49]. This fact brings some difficulties in the estimation of the conduction band offsets, also necessary to depict a band diagram of the heterojunction, as it is not clear how the chemical bath used for the buffer deposition affects the surface structure of the absorber during the first stages of the process. In particular, if Na plays a role in the surface energy band gap enlargement, values of the surface energy gap closer to those reported for the film bulk are to be expected after few seconds processing in the chemical bath, due to Na removal in the solution, as mentioned above. If, on the other hand, the large band gap results from structural disorder, the values obtained from the inverse photoemission studies can be included in the calculation. We will return to this point after completing the calculation of the valence band offset.

Values of energy differences between core level binding energies and the valence band edges, as well as energy differences between core level pairs of both CGSe and CdS compounds, are summarised in Table 5. From these results, and according to Eq. 118, a valence band offset $\Delta E_V = -1.0\pm0.2$ eV is estimated for the CGSe/CdS interface, where the negative sign denotes a downward shift when transiting from the CGSe to the CdS. These results are in good agreement with those reported by Nadenau[186], where a valence band offset of -0.9 eV was calculated for the CGSe/CdS interface following the same procedure on PVD-grown absorbers. Slight differences are found with values of binding energies reported in Ref. [186], that can be attributed to the fact that samples in the present study were preserved against air exposure. Nevertheless, the reasonable agreement (within the accuracy limits of the method) in final results leads us to conclude that effects related to a brief exposure of the absorber film to ambient conditions have little impact on the subsequent device processing, as the chemical bath provides a convenient surface conditioning prior to the actual buffer deposition. Furthermore, these results also exclude any influence (either positive or negative) on device processing of characteristic issues of the CVD process, concretely the presence of iodine at the CGSe surface, as similar results to the case of PVD processed absorbers of Ref. [186] have been found.

Table 5. Energy differences between core levels and valence band maximum (E_{CL}-E_V) of CGSe and CdS elements. Energy differences between core level pairs from both materials, ΔE_{CL}(CGSe-CdS), are also included, as well as calculated values of the valence band offset (ΔE_{CL}) for each core level pair. The negative sign means a downward shift when transiting from CGSe to CdS. All energies given in eV.

Core level	E_{CL} - E_V	ΔE_{CL}(CGSe-CdS)			Core level pairs, calculated ΔE_V	
Cd 4d	9.2±0.1		Cd 4d	Cd 3p	Ga 3d/Cd 4d	-1.0±0.2
Cd 3p	616.9±0.1	Ga 3d	8.7±0.1	-599.0±0.1	Ga 3d/Cd 3p	-1.0±0.2
Ga 3d	18.9±0.1	Se 3d	43.1±0.1	-564.6±0.1	Se 3d/Cd 4d	-1.0±0.2
Se 3d	53.3±0.1				Se 3d/Cd 3p	-1.1±0.2

The CGSe/CdS interface has also been analysed by means of electron microscopy, in order to gain some insight into the structural quality of the interface. HRTEM images of the CGSe/CdS interface of two-stage based samples after standard device processing, like the one shown in Figure 63, show a well defined border between the absorber and buffer films, as stated above one of the major requirements for the application of Anderson's model to the heterojunction problem. Furthermore, two phases of CdS have been found from the analysis of Fourier transform pictures and lattice plane spacing in different domains of the buffer layer, in agreement with previous results on the characterisation of CBD deposited CdS[186]. Cubic CdS (JCPDS 10-454) crystallises in the zincblende structure, with a lattice constant of 5.8 Å, whereas hexagonal CdS (JCPDS 41-1049) crystallises in wurtzite structure, showing a basal plane lattice constant a=4.1 Å and c=6.7 Å. Considering the basal plane lattice constant of CGSe a=5.6 Å, simple estimations of the lattice mismatch at the heterojunction between CGSe and CdS read 3.5 % for the case of zincblende phase. For the hexagonal modification of CdS, the mismatch factor will depend on the particular facets of both species brought in contact. Nadenau[186] estimated this value to have a minimum ~4 % for $(112)_{CGSe}/(001)_{CdS}$.

Highly defective regions in the buffer layer can be identified in Figure 63 close to the heterojunction, which can be attributed to the lattice mismatch. This is expected to have a direct impact on the electronics of the junction, as it will be discussed in the next sections. Additionally, a near surface region within the CGSe absorber presents a less defined ordering, compared to the inner part on the right side of Figure 63, where (112) planes are inferred from the spacing (d=3.44 Å). The disordered region extends over the last few nm of the absorber thickness, forming the junction with the CdS buffer layer. These observations support the attribution of the surface band gap enlargement to a disordered phase of the CGSe. However, it can not be excluded that this is to some extent the result of the action of the chemical bath, that may act as a soft etching agent during the first stages of the deposition process, as pointed out earlier.

Based on these observations, and taking into account the results of the photoemission study of the valence band offset, two different possibilities will be contemplated for sketching the CGSe/CdS band diagram. The first assumes that the CGSe bulk value of the band gap (E_g=1.65 eV as inferred from quantum efficiency, see Section 4.2) is valid at the surface, due to the cleaning effect of the chemical bath. Disorder and/or surface phases of CGSe with different material properties are thus excluded in this model. From this, it follows that the conduction band offset would result in a cliff at the interface, amounting for 0.25 eV, as depicted in Figure 64.

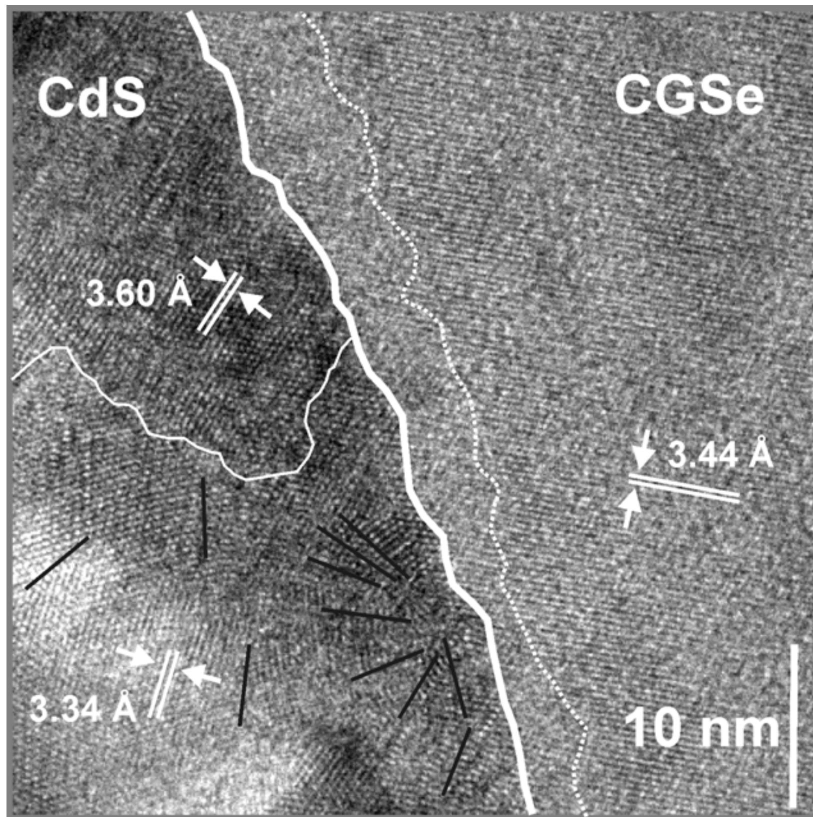

Figure 63. HRTEM image of the CGSe/CdS interfacial region of a two-stage based solar cell. The thick white line highlights the heterojunction between both materials. The thin white line isolates an hexagonal domain within the CdS buffer layer in the upper left part. Cubic CdS forms the lower left part of the buffer. Straight lines are a guide to the eye on line defects, dislocations, and low angle grain boundaries, especially abundant within the cubic domain of CdS. The CGSe region between the interface and the white line presents a less defined ordering than the inner side of the crystallite, on the right.

The second possibility includes a near-surface CGSe layer with a higher band gap than the bulk, resulting from structural disorder and/or the soft etching action of the chemical bath. It is assumed that the maximum band gap enlargement can be that reported by Meeder[50] on bare absorbers from two-stage processes (E_g=2.0 eV). Furthermore, the band gap enlargement at the surface of Cu-poor chalcopyrites is expected to result from a lowering of the valence band in the energy scale, without significant modifications of the conduction band. This is due to the active role played by Cu-d levels in the structure of the valence band, as discussed in Chapter 1, whereas conduction band states are mostly provided from Se and Ga states[32]. The conduction band offset resulting from this model is an enlarged cliff of 0.6 eV, as also shown in Figure 64.

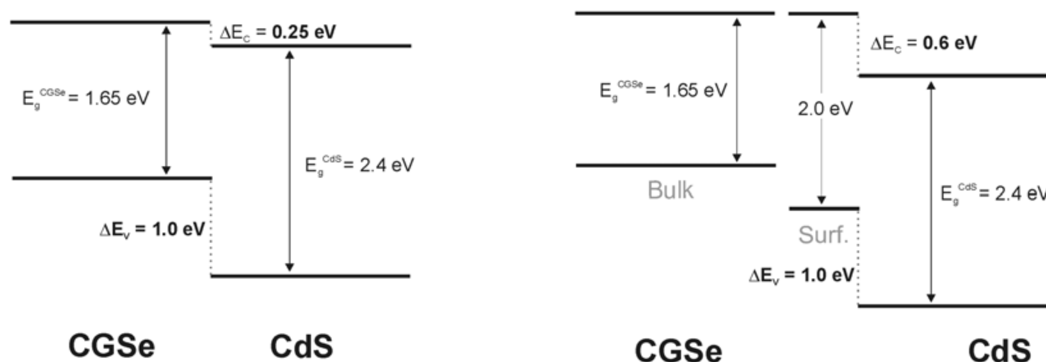

Figure 64. Proposed band alignment schemes for the CGSe/CdS interface, excluding band bending. **(Left)** E_g^{CGSe} bulk value assumed to be valid at the CGSe surface. **(Right)** CGSe surface layer with enlarged band gap (following Meeder *et al.*[50]) mediating the interface.

It is presumed that the actual situation in CGSe-based devices lies somewhere in between these two cases. Qualitatively, the two models are similar regarding PV performance, as open-circuit voltage losses are predicted in both cases due to the presence of cliffs at the conduction band, the height of the cliff determining the extent of the losses in each case, in agreement with experimental results[195] and numerical calculations[179]. However, the near-surface lowering of the valence band with respect to the bulk can have an effect on the recombination mechanisms across the junction, as the potential barrier E_A for interface recombination, as defined in Section 2.2.1.1, increases[196]. Whether this barrier height is enough or not to prevent interface recombination, will be discussed in Section 4.3.

The minor band bending at the CGSe/CdS interface, as recorded from photoemission experiments, would not result in an operating device, if these were the only compounds involved in the heterojunction. Most of the built-in potential in actual devices (V_{bi}>840 mV, according to the obtained values of Figure 51 from the KPFM work function measurement on cross sections) results from the subsequent deposition of the highly doped ZnO window layer over the buffer. Values of the corresponding band offsets for the CdS/ZnO interface have been reported[197] on the basis of UPS studies (with CdS overlayers evaporated on ZnO substrates) as ΔE_V=-1.2 eV and ΔE_C=-0.3 eV, where negative signs indicate that the VB maximum and CB minimum of ZnO are lower than the corresponding CdS band edges.

4.2 Quantum efficiency and EBIC

Quantum efficiency measurements have been performed on samples from single- and two-stage processes, as well as on samples processed on Cu-precursors, in order to monitor the effects on the electronic quality of the junction resulting from the modified recipes. Figure 65 shows external QE measurements of single and two-stage based devices under different applied bias. These values have been corrected for series resistance effects following the procedure stated in Chapter 1. An improved carrier collection can be observed in the two-stage sample over the entire wavelength range

compared to the single stage based device, as can be inferred from the reduced collection losses at long wavelengths (λ>550 nm) schematically indicated in Figure 17. Additionally, the QE yield extends up to longer wavelengths (~780 nm) in two-stage samples, indicating a narrower mobility gap compared to the case of single stage samples.

An analysis of differentiated QE curves helps quantify differences in energy gaps between single and two-stage processed samples. Peaks in Figure 66 correspond to the different energy band gaps in the wavelength range of interest, those lowest gaps of ZnO, CdS and the three pronounced gaps of CGSe. A shift of nearly 20 meV in the lowest CGSe band gaps to lower energies is found in the case of two-stage samples. Similar results have been found by Schuler[66] for Ga-rich PVD-grown CGSe films. The decrease in the energy gap with off-stoichiometry towards Ga-rich compositions (characteristic of two-stage samples, as discussed in Chapter 3) is interpreted as a result of the structural disorder, and is in agreement with optical absorption measurements performed on single and two-stage samples grown on bare glass substrates[128].

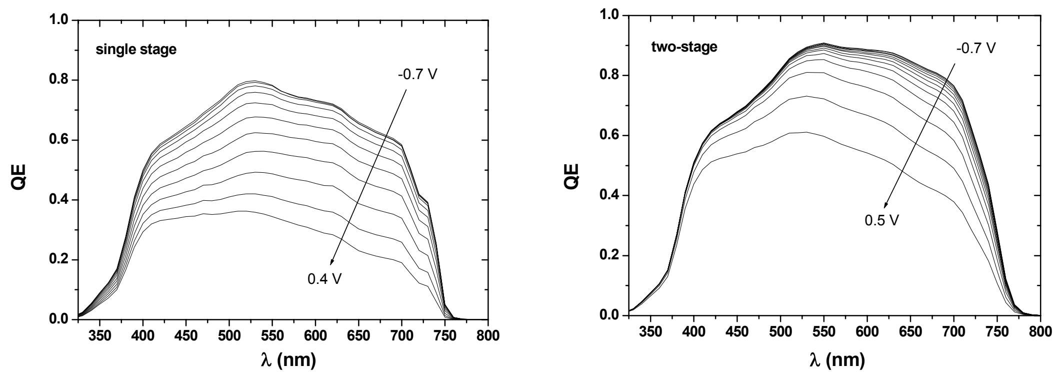

Figure 65. External QE (corrected for series resistance) of single **(left)** and two-stage CVD-based CGSe thin film solar cells **(right)**, for different biasing conditions (reverse to forward bias, 0.1 V steps).

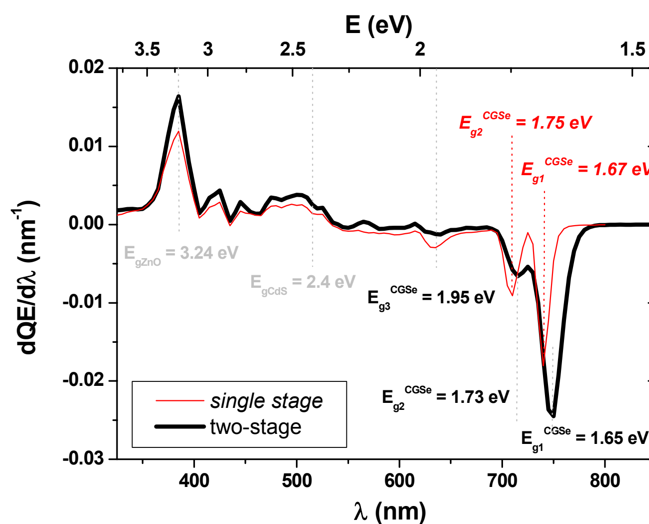

Figure 66. Differentiated values of QE over exciting photon wavelength (lower axis) and energy (upper axis) of single and two-stage samples from Figure 65 (zero bias). Values of lowest energy band gaps are given for ZnO and CdS, as well as those of the three lowest gaps of CGSe.

Following Eq. 101, quantitative information on the minority carrier diffusion length can be obtained from QE plots. Figure 67 shows the long wavelength range of the QE measurements performed on single and two-stage samples for three selected biasing conditions, and the corresponding fitting values with the given effective diffusion lengths. Single-stage based devices are characterised by low values of the effective diffusion length, above half a micron at zero bias, as well as by a large effect of biasing conditions on the QE yield. These two observations are related to the same effect, namely a narrow depletion region, whereby any modulation of the SCR width with the applied bias will influence noticeably the value of the effective diffusion length and thus the collection efficiency.

Values of L_{eff} above 1μm are obtained from the fits for the case of two-stage based devices at zero bias, with a minor effect of biasing on the QE yield. This can be seen in Figure 68, where values of QE at a wavelength of 700 nm are shown under biasing conditions for a second pair of single and two-stage based devices. Solid curves correspond to polynomial fits of the QE as a function of the applied bias, showing a good agreement with a quadratic dependence in the case of single stage devices, as would be expected from Eq. 103 and the modulation of the SCR width with the external bias. However, a slower varying function (fitted with a fourth-order polynomial) is found in the case of two-stage processed devices. This suggests a fundamental difference in the bias dependence of the SCR width on the applied bias, assuming that the actual diffusion length of the minority carriers is in turn bias independent. Second-order terms in the w(V) relation should therefore be included in Eq. 103 to preserve the expected dependence. On the other hand, charge and discharge of interface states may occur as a function of the applied voltage, including an additional bias dependence of the SCR width through the density of interface states in Eq. 103, implicitly assumed to be constant, that can account for the observed w(V) relation.

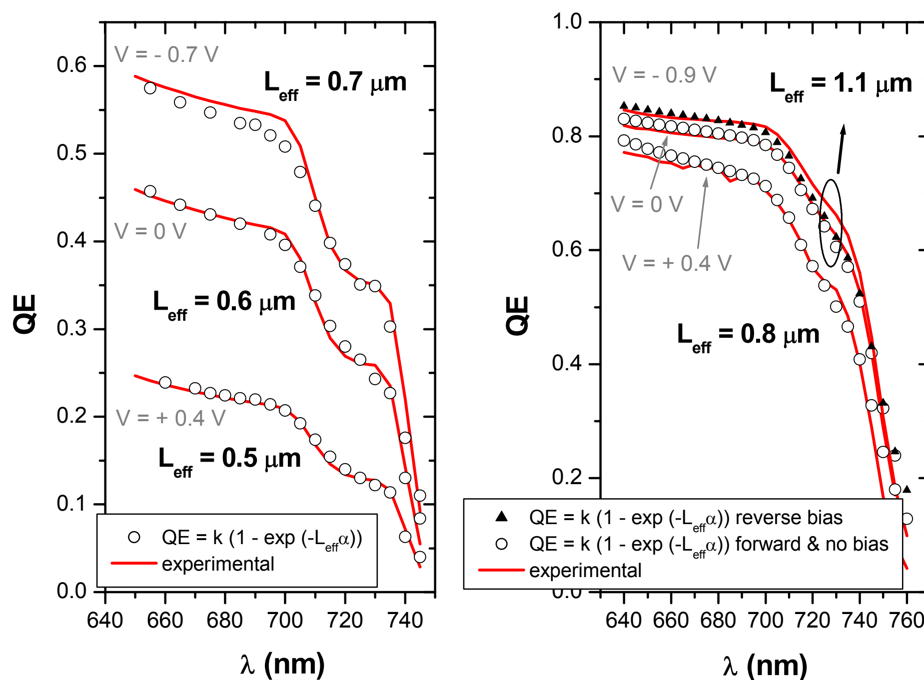

Figure 67. QE measurements and fits of single- (left) and two-stage (right) samples under voltage bias and corresponding effective diffusion lengths, as calculated from Eq 101.

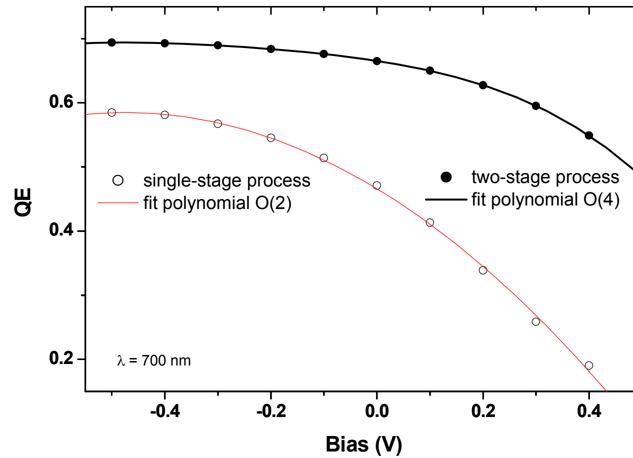

Figure 68. Bias dependence of QE values at λ=700 nm for single and two-stage based devices, with corresponding polynomial fits.

Due to the different behaviour of both types of samples with the applied bias, it turns out inconvenient to apply the method exposed in Chapter 2 for the separation of the minority carrier diffusion length and the SCR width. This approach was followed by Schuler[66] in order to discern effects on CGSe/CdS heterojuctions resulting from different CBD deposition processes. Alternatively, a direct comparison of the parameters can be made from EBIC studies, based on the analysis described in Chapter 2. Normalised EBIC profiles and the corresponding collection functions of minority carriers as a function of the position in the device are shown in Figure 69 for a pair of samples from single- and two-stage absorbers. Parameters used for the collection efficiency fits, as described in Chapter 2, are recorded in Table 6.

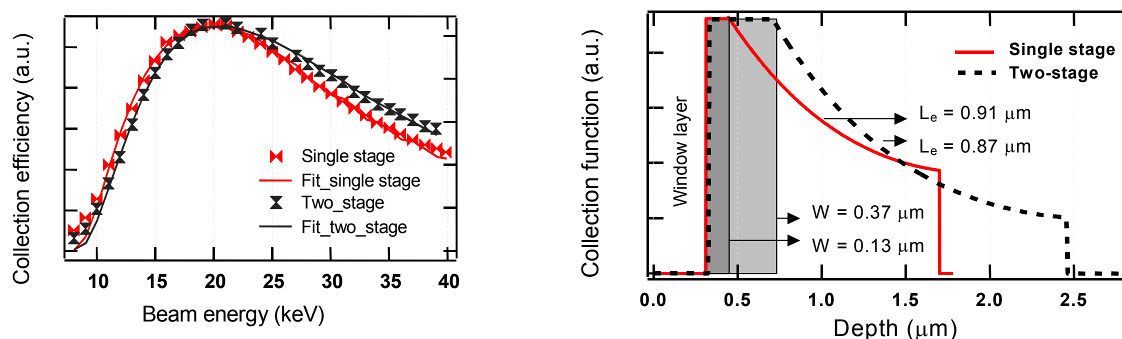

Figure 69. (Left) Collection efficiency as a function of the electron beam energy as measured from EBIC on single and two-stage samples and corresponding fits with the parameters given in Table 6. **(Right)** Collection function and corresponding values of the SCR width w and minority carrier diffusion lengths L_e calculated from the fits.

From the calculated collection function profiles, it can be concluded that the main contribution to the increased effective diffusion length of minority carriers in two-stage based absorbers results from the enlargement of the SCR width. Similar values are

obtained for the actual electron diffusion lengths, an interesting result by itself, as it states that minor disturbance to the electronic diffusion in the absorber bulk is introduced during the second stage of the sequential growth process. The enlargement of the SCR width in the absorber is interpreted as the result of a reduced net doping density compared to the case of single stage samples, possibly related to the nearly intrinsic surface layer depicted in Figure 64. Additionally, a reduced amount of interface states will widen the SCR, according to Eq. 103. This possibility will be evaluated in the next section, where recombination mechanisms in both types of devices will be assessed.

Table 6. Parameters used for the fit of EBIC profiles included in Figure 69, and values obtained for the diffusion length and SCR width of single and two-stage samples.

Parameter		Single stage	Two-stage
Absorber density	(g/cm^{-3})	5.45	5.45
Window density	(g/cm^{-3})	5.60	5.60
Absorber thickness	(μm)	1.40	2.14
Window thickness	(μm)	0.31	0.33
Diffusivity	(cm^2/s)	1	1
Surface recombination velocity	(cm/s)	3.3	3.3
Diffusion length	*(μm)*	*0.91±0.05*	*0.87±0.05*
SCR width	*(μm)*	*0.13±0.05*	*0.37±0.05*

The significant improvement of the effective diffusion length figures in devices based on two-stage processing is the most direct experimental proof of the higher absorber quality achieved by this growth method. Generally, higher minority carrier collection efficiencies are achieved from slightly Ga-rich materials, including those grown in single stage processes. However, the composition criterion is not sufficient to design a high efficiency device, as both optical and electronic losses will limit the performance in absorber layers below 1 μm thickness and with numerous grain boundaries along the path minority electrons must diffuse through in order to reach the p-n junction, both aspects being characteristic of Ga-rich single stage samples. These difficulties are overcome in two-stage grown absorbers, as discussed in Chapter 3.

Devices based on Cu-precursors (either annealed in Ga- and Se-rich atmosphere or fully processed following a two-stage recipe, as explained in Chapter 3) show similarities to the case of single-stage based samples. A wide modulation of the quantum yield results from changes in the voltage bias, both in forward and reverse conditions. In the case shown in Figure 70, based on a two-stage process on a 200 nm thick Cu-film, slightly higher values were obtained for the effective diffusion length, compared to those from the single stage sample in Figure 67. In agreement with this observation, these type of devices show comparably slightly higher short-circuit currents than devices based on single stage samples, being mainly limited by poor fill factors and open-circuit voltages, as discussed in the next section.

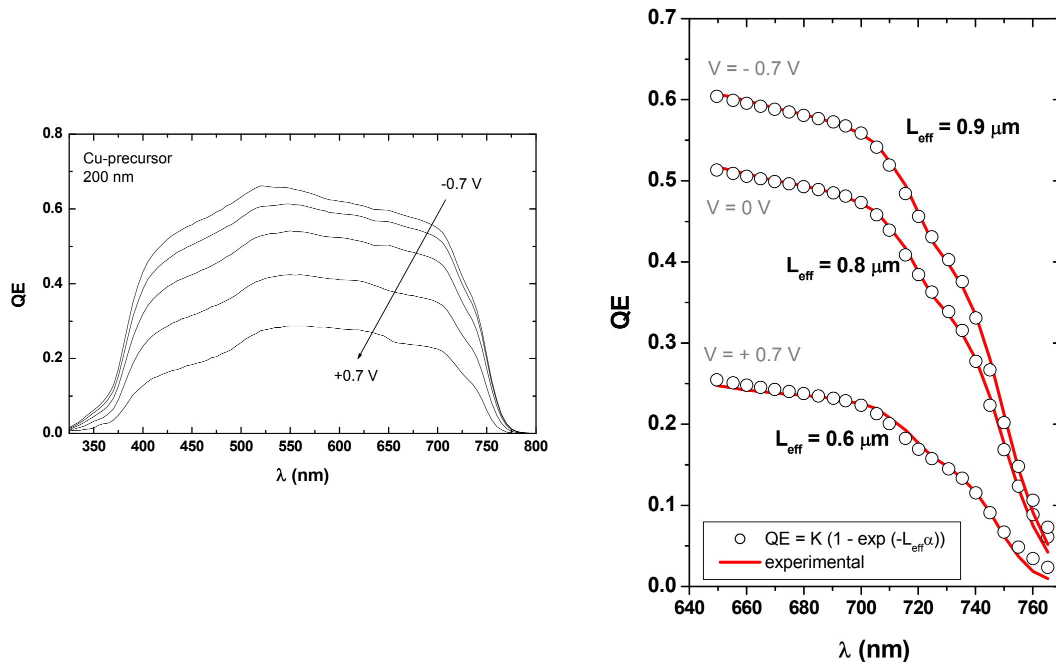

Figure 70. Experimental QE **(left)** under bias (0.35 V steps) and extended view on the long wavelength range **(right)** including fitted values and effective diffusion length figures, of a 200 nm thick Cu-precursor sample (two-stage process).

4.3 I(V, T) analysis

Current-voltage characteristics have been measured on samples based on different types of CVD-grown CGSe absorbers, processed from single- and two-stage recipes and Cu-precursors. The measurements were performed in the sun simulator to monitor their performance under standard conditions and in the I(V,T) set up described in Chapter 2, in darkness and under illumination. As discussed in detail in Section 2.2.1, measurements conducted in darkness provide direct information on the quality of the p-n junction, whereas measurements under illumination simulate the real operation of PV devices under working conditions. It is of special interest to monitor changes in the electronic transport between these two cases, in order to infer what limiting factors play a role in the device performance. In particular, the impact of interface recombination at the p-n junction is of critical importance regarding the optimisation of standard CdS buffer layer recipes and/or its possible substitution by e.g. environmentally friendly (Cd-free) alternatives.

Figure 71 shows dark J-V curves at room temperature of two batches of single and two-stage based devices. In the case of single stage devices, the samples included in the figure were processed on CGSe absorbers with [Ga]/[Cu](s) ratios between 1.0 and 1.1, as measured by EDX. Within this composition range, it is found that improved diode J-V characteristics are obtained with increasing Ga-content in the absorber films. This is concluded from the downward shift of the entire curves to lower values of the current density axis, indicating an increase of shunt resistance values, thus reducing leakage currents, as discussed in Chapter 2. The linear range in the semilogarithmic plot of the

J-V curves for medium forward bias corresponds to the diode transport, as indicated in Figure 11. In Figure 71 (left), it is observed that wider ranges of linear relationship of the current density over the applied forward bias are accessible for Ga-rich compositions, indicating an extended range of diode-controlled electronic transport. Effects attributed to series resistance are visible on the high forward bias range, which will deserve some attention in the further discussion.

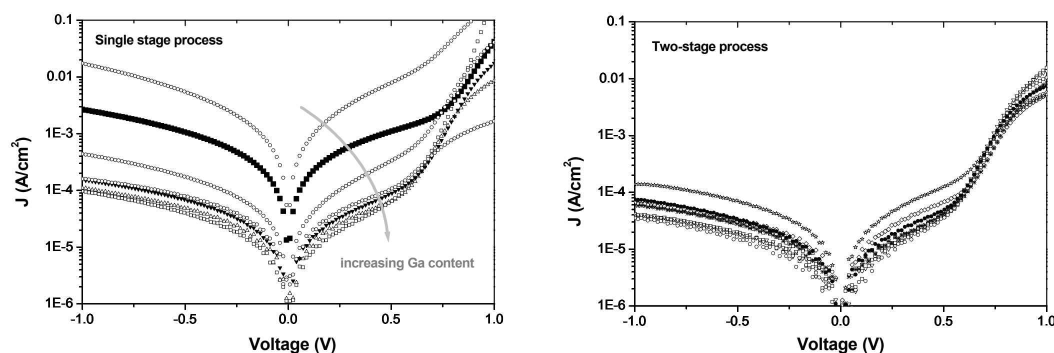

Figure 71. Dark J-V curves at room temperature of single-stage based samples with various absorber compositions **(left)** and of two-stage based devices **(right)**.

In comparison to samples processed from single stage absorbers, two-stage samples included in Figure 71 (right) show dark J-V curves qualitatively comparable to those from single stage Ga-rich absorbers, as expected from composition ratios [Ga]/[Cu](s)>1.2 of the CGSe absorber films, from EDX measurements. The scatter in current values can be considered as an indication of the process reproducibility, as the same standard recipe (see Appendix I) was used for all samples included in the figure.

Figure 72 shows a comparison of typical dark J-V curves (forward bias branches) of single- and two-stage devices measured at room temperature. Experimental data and fitted values according to the single diode model proposed in Chapter 2 are included in the plot, together with the corresponding fitting parameters. From these values, the main features of the electronic transport expected on both types of devices can be outlined:

- A significant decrease of nearly three orders of magnitude is recorded in the saturation current values on samples processed following two-stage recipes. The thermal generation and recombination of free carriers responsible of the saturation current is greatly assisted by the presence of deep defect levels within the energy band gap of the absorber film. It has been shown that single-stage processed CGSe films are characterised by a high sub-band gap absorption, resulting from a high density of electronic states in the gap[128]. This absorption is greatly reduced after processing the second stage of the film growth, constituting a major improvement of the sequential deposition recipe on the film quality, and consequently on the device performance.

- Ideality factors above 2 are commonly found from the fits of dark J-V curves of single-stage based devices, pointing to tunnelling-enhanced recombination processes dominating the electronic transport. On the other hand, values of the ideality factor close to 2 are found in two-stage based

devices, which are in agreement with thermally activated recombination processes. The confirmation of these statements must follow from the study of the ideality factor temperature dependence, as outlined in Chapter 2, that will be discussed in the following.

- Higher values of the shunt resistance R_{sh} are achieved in two-stage based devices compared to those based on single stage samples (this aspect also depending on the [Ga]/[Cu] ratio of single stage samples, as seen in Figure 71), resulting in reduced leakage currents. Higher open-circuit voltages and fill factors can in principle be expected from two-stage devices under operating conditions.

- Remarkably large values of the series resistance (above 10 Ωcm^2) are obtained from the fits of dark J-V curves from two-stage devices, readily visible from the high forward-bias range of the curves included in Figure 71 (right). On the other hand, a large scatter in the corresponding values of single stage devices is found, including values comparable to those of two-stage samples, as well as reduced values like in the case shown in Figure 72. In general, increasing the Ga-content of single stage samples results in an enhancement of the effects related to the series resistance, although exceptions are found.

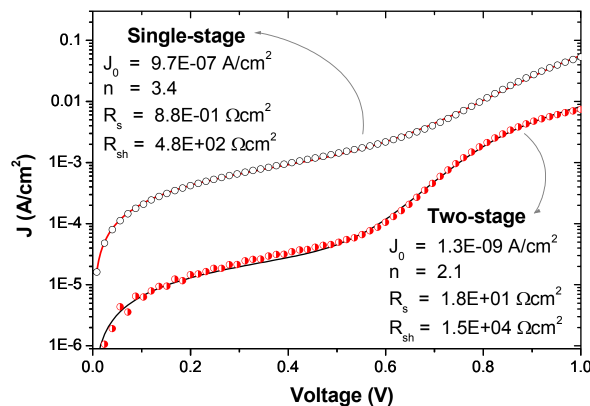

Figure 72. Forward bias branch of dark J-V curves at room temperature of representative devices from single and two-stage based absorbers. Experimental data (dots) and corresponding fits (solid lines) with the given parameter values are included.

Such high values of the series resistance should in principle result in poor fill factors, short-circuit currents, and correspondingly low efficiencies, as it is shown in Figure 73 from simulated J-V curves of a typical $CuInSe_2$-based solar cell[96] with different values of R_S. Surprisingly, the expected tendency is not found when plotting the PV parameters of operating devices over the series resistance values obtained from dark J-V fits, as it can be seen in Figure 74 for the efficiencies of various samples from single and two-stage devices. Devices showing fitted values of the series resistance as high as 100 Ωcm^2 still yield efficiencies around 3.5%. These considerations put in question the attribution of the experimental J-V results for high forward bias solely to a simple linear

term in the single diode model, according to Figure 10 and Eq. 50 in Chapter 1. Further evidences in this direction will be found from the J(V, T) study.

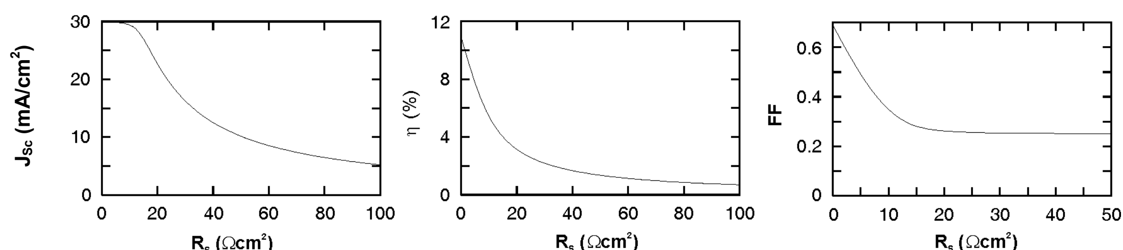

Figure 73. Calculated values of the short-circuit current, efficiency and fill factor as a function of the series resistance of a typical $CuInSe_2$-based thin-film solar cell at room temperature. (Adapted from Ref. [96]).

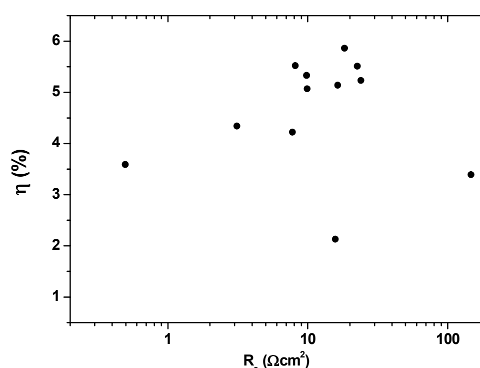

Figure 74. Values of the experimental efficiency as a function of the fitted series resistance from dark I-V measurements from various CVD-grown CGSe-devices from single- and two-stage processes at room temperature.

J-V measurements were performed in the sun simulator at room temperature under AM1.5G illumination conditions. Figure 75 shows the absolute value of the current density in linear scale over the applied bias, for the two sets of single and two-stage samples included in Figure 71. Whereas minor improvements are recorded in the open-circuit voltage of two-stage samples, compared to those from single stages, higher figures of short-circuit current density (highlighted in the figure) and fill factor are readily visible. These results are in agreement with previous QE results, following the discussion presented in Chapter 2, as large effective diffusion lengths are associated to an improved collection of minority carriers contributing to the photocurrent.

Table 7 summarises the PV parameter values obtained from the best solar cells (i.e. highest efficiency) based on the growth processes assessed in this study, together with the maximum values of a single parameter recorded from different cells. Single stage based samples are used as reference, to which values from samples based on modified recipes are compared. Open-circuit voltages above 800 mV are accessible from any of the three approaches considered.

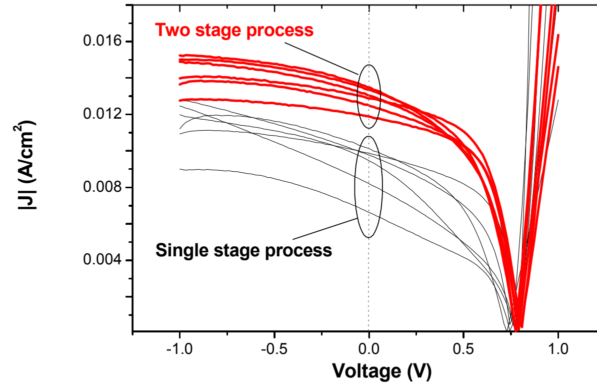

Figure 75. Illuminated (AM1.5G) |J|-V curves of single and two-stage based CGSe devices at room temperature.

Table 7. Highest PV parameter values of thin-film solar cells based on CVD-grown CGSe from different types of absorber deposition process. *Best cell* refers to the device with highest efficiency from each type of process. *Max.* corresponds to the highest value of a single parameter obtained from samples of each type of process.

Process	**V_{OC} (mV)**		**FF**		**J_{SC} (mA/cm^2)**		**η (%)**	**Comments**
	Best cell	**Max.**	**Best cell**	**Max**	**Best cell**	**Max.**		
Single stage	781	*863*	0.58	*0.58*	9.9	*10.4*	**4.5**	
Two-stage	818	*844*	0.62	*0.62*	14.2	*14.2*	**7.2**	↑J_{SC}, ↑FF
Cu-precursor	817	*817*	0.54	*0.54*	9.9	*12.0*	**4.2**	2-stage ↑J_{SC}, ↓FF

In order to determine the limiting factors of the device performance, J-V characteristics have been measured as a function of the temperature and illumination intensity in the I(V, T) set-up. Figure 76 shows semilogarithmic plots of dark and illuminated curves (the latter based on J_{SC}-V_{OC} values, as discussed in Section 2.2.2) of solar cells processed on CGSe absorbers from single-, two-stage and a 200 nm thick Cu-precursor, the latter fully processed following a sequential deposition recipe (see Section 3.4.2.1).

Bearing in mind the characteristic dependences of the experimental J-V characteristics on the parameters from the single diode model, as depicted in Figure 11, differences between dark J-V curves shown in Figure 76 can be attributed to dissimilar contributions from the shunt resistance, the saturation current and the diode ideality factor on each type of cell. Whereas the effect of shunt resistance R_{SH} is minimised in the case of two-stage processed samples, low R_{SH} values are found in samples based on Cu-precursors, shifting the J-V curves to higher current values in the low forward bias range. Furthermore, the linear range corresponding to diode-controlled electronic transport in Cu-precursors is limited only to high temperatures (T>300 K), indicating the dominance of alternative paths in the electronic transport, in agreement with low R_{SH} values. Similar effects are found in the corresponding J_{SC}-V_{OC} curves. Deviations from linearity in the high-bias range of the semilogarithmic J_{SC}-V_{OC} plot prevent the application of the I(V,T) analysis introduced in Section 2.2.2 at low temperatures on samples based on Cu-precursors, regarding the study of temperature dependence of the

ideality factor and the activation energies of the corresponding saturation currents, which will thus not be included in the following discussion.

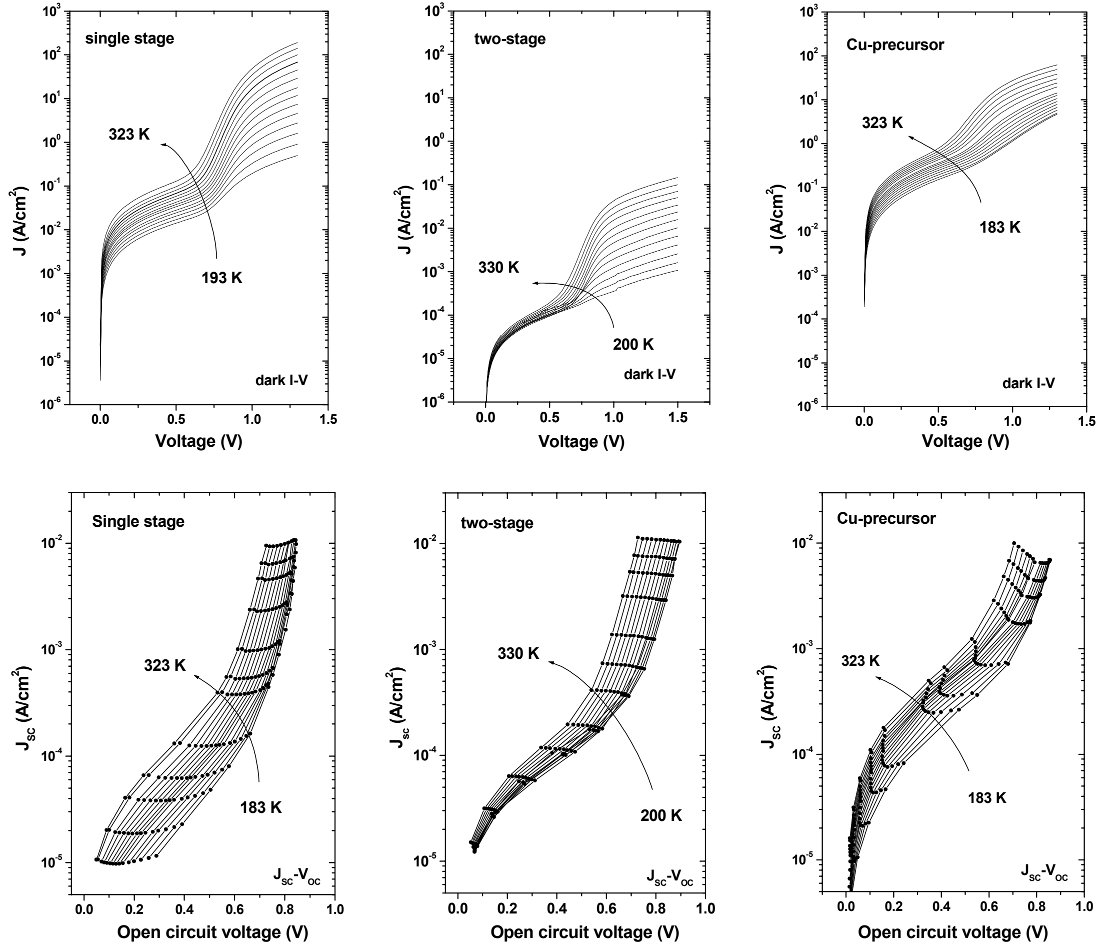

Figure 76. (Upper) Semilogarithmic plot of the forward bias branch of dark I-V curves from single-, two-stage- and Cu-precursor-based CGSe solar cells recorded at different temperatures. **(Lower)** Corresponding J_{SC}-V_{OC} plots of the same samples.

Corrected Arrhenius plots of the saturation current over the inverse temperature have been obtained from single and two-stage based devices, as shown for a pair of samples in Figure 77 (left). The plot shows as y-axis the product of the ideality factor times the saturation current density, in order to account for the temperature dependence of the ideality factor, as derived from Eq. 66:

$$A \ln J_0 = -\frac{E_A}{kT} + A \ln J_{00} \qquad \text{Eq. 119}$$

where E_A is the activation energy defined in Section 2.2.2 and the last term is a slow varying function of the temperature[198]. According to this expression, a linear dependence of the product $A\ln J_0$ over the inverse temperature is predicted, with slope E_A/k. Activation energies of the saturation current from single- and two-stage based

devices in darkness and under illumination are included in Figure 77. These values were obtained from the fit of corrected Arrhenius plots in the high temperature range, as deviations from the diode-controlled transport regime appear at low temperatures, being specially significant in dark I-V curves (see Figure 76).

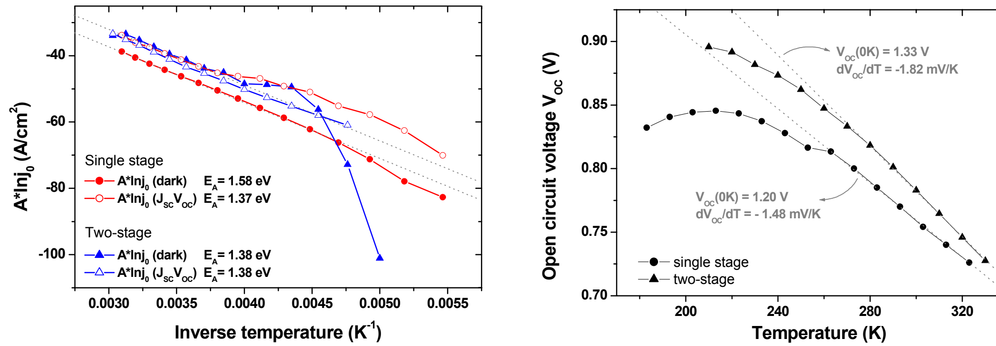

Figure 77. (Left) Corrected Arrhenius plots of the saturation current over the inverse temperature of single and two-stage based CGSe devices in darkness and under illumination, and corresponding activation energies obtained from the linear fit of the curves in the high temperature range. **(Right)** Temperature dependence of the open-circuit voltage of single- and two-stage based devices, with extrapolated values at 0K.

Both types of samples are dominated by interface recombination, as inferred from values of the activation energy E_A<E_g, and according to the results summarised in Table 1. This is confirmed by the extrapolated value of the open-circuit voltage V_{OC} at T=0K of both types of samples, shown in Figure 77 (right), in good agreement with the activation energy of the saturation current and clearly lower than the corresponding energy band gaps (E_g=1.65-1.67 eV from quantum efficiency measurements, see Figure 66) of single- and two-stage absorbers, thus excluding SCR-based recombination. Remarkably, a change in the activation energy of single stage samples is recorded from E_A=1.58 eV to E_A=1.37 eV comparing the measurements performed in darkness and under illumination. According to the model presented in Section 2.2.2, the activation energy of the saturation current expected from devices dominated by interface recombination is related to the potential barrier that holes diffusing from the absorber bulk must surmount in order to recombine with electrons from the window at the interface. A reduction of the activation energy is thus associated with a lowering of the potential barrier for holes (i.e. a decreased band bending at the heterojunction under illumination), favouring interface recombination at the CGSe/CdS interface. The activation energy value in the case of dark measurements is low to attribute the main recombination current contribution to thermally activated SCR recombination, thus also indicating interface-dominated recombination in this case. The measured difference in activation energies is thus attributed to changes in the electric charge stored at interface states as result of illuminating the junction, rather than to a change in the main recombination mechanism controlling the electronic transport in the device.

Contrarily to the case of single stage samples, no change in the activation energy of the saturation current is found in two-stage based devices under different illumination conditions. The same value E_A=1.38 eV is obtained from dark and illuminated I-V

curves, indicating that no major change in the electronic transport takes place in the device under operating conditions, again attributed to interface recombination from the agreement between the activation energy and the extrapolated open-circuit voltage at T=0K. The constancy of the activation energy value points to the pinning of the quasi-Fermi level of holes at the interface, thus maintaining the same potential barrier for their recombination at the interface with electrons from the window under illumination. This can be attributed to a high density of interface states, as inferred from the highly defected near surface regions both in the absorber and buffer films identified by TEM studies (see Figure 63), a fact that can also explain the distinct bias dependence of the quantum efficiency found in two-stage based devices, discussed in Section 4.2.

The temperature dependence of the diode ideality factor contains information about the type of process conducting the recombination, either thermal activation or tunnelling. Figure 78 shows the ideality factor of single and two-stage samples as a function of the temperature, both in darkness and under illumination. Values A>2 are recorded in all cases within the studied temperature range, pointing to tunnelling enhancement of the interface recombination, according to the results presented in Table 1. Slight differences are found when comparing the behaviour of single- and two-stage based devices, which can be related to those differences found in the activation energy of the saturation current. In the case of single-stage devices, tunnelling enhancement appears more significant in the case of measurements performed in darkness, as inferred from the stronger temperature dependence of the ideality factor in this case. This result is in agreement with a steeper band bending (and thus a higher electric field associated) within the SCR of the absorber film, concluded from the larger potential barrier for the activation of interface recombination proposed for the case of measurements conducted in darkness. Fitted values of A(T) according to the general expression for tunnelling enhanced interface recombination (see Table 1):

$$A(T) \propto \frac{E_{00}}{kT} \coth\left(\frac{E_{00}}{kT}\right) \qquad \text{Eq. 120}$$

are included in Figure 78 (left) for two values of the characteristic tunnelling energy E_{00}. The analytical expression for E_{00} in the case of an ideal Schottky contact reads[199]:

$$E_{00} = \frac{q\hbar}{2}\sqrt{\frac{N_A}{m^* \varepsilon\varepsilon_0}} \qquad \text{Eq. 121}$$

where m^* is the effective tunneling mass, $\varepsilon\varepsilon_0$ is the dielectric constant of the material and N_A is the net (hereafter referred to as the *effective*) doping concentration of the absorber, which in the original model from Padovani and Stratton[199] is the only material parameter determining the associated band bending of the heterojunction (i.e. excluding surface states and charge storage at the interface, in the so-called Schottky limit[183] of a metal-semiconductor junction).

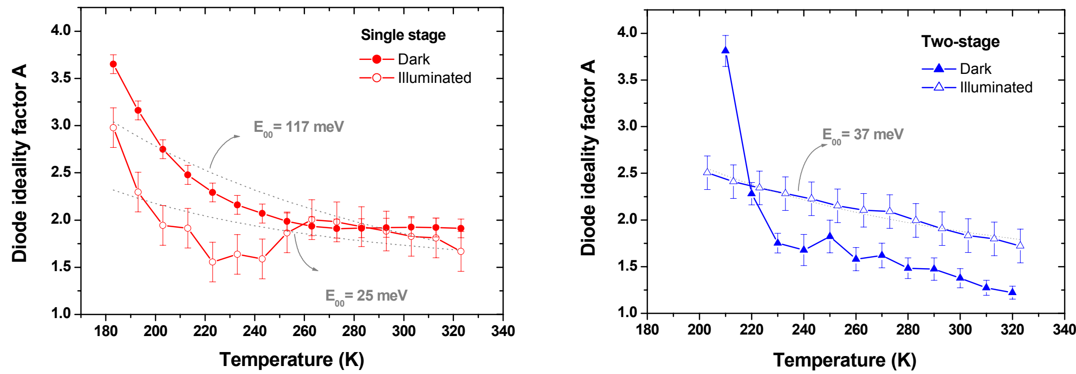

Figure 78. (Left) Temperature dependence of the ideality factor of a single-stage-based CGSe device in darkness and under illumination. Dotted lines correspond to the expected values assuming tunnelling-enhanced interface recombination with characteristic tunnelling energies E_{00}= 25 meV and E_{00}= 117 meV. **(Right)** As before, for the case of a two-stage-based CGSe device, and corresponding fit with E_{00}= 37 meV.

Higher *effective* doping concentrations (by approximately a factor 20) are deduced from the measurements conducted in darkness, when comparing the tunnelling energies recorded in Figure 78 to the case of measurements performed under illumination, assuming a constant effective mass for tunnelling. This change in *effective* doping concentration is actually not related to any change in the absorber net doping concentration, as would follow from Padovani's model, but linked to a simultaneous change in the amount of charge stored at the interface, as stated in Eq. 95 and discussed in Section 2.2.3. It is concluded that illuminating the junction of single-stage-based devices increases the concentration of interfacial charge located at acceptor-like states by trapping photogenerated electrons. This results in a reduced band bending on the absorber side of the junction, and consequently in a reduced potential barrier for the activation of interface recombination. The effect of increasing the interface charge at the CGSe/CdS junction on the band diagram for a given net doping concentration of the absorber film has been simulated numerically with the help of the software package SCAPS [(200]. Material parameters used for the simulation are given in Appendix II. Figure 79 shows the reduction of the band bending associated to the absorber film upon increasing the density of charged acceptor-like interface states from 10^{10} cm^{-2} to $5 \cdot 10^{12}$ cm^{-2} for a CGSe-based device in equilibrium. The simple band diagram given in Figure 64 (left), i.e. excluding the presence of the surface phase with enlarged band gap in the absorber film, has been considered for the sake of clarity in the resulting diagram while performing these simulations, although similar results were recorded when including the surface phase at the CGSe/CdS interface, as depicted in Figure 64 (right). A net reduction of the band bending in the CGSe depletion region ΔE_A is recorded, in agreement with the associated reduction of the activation energy of interface recombination (see Figure 14).

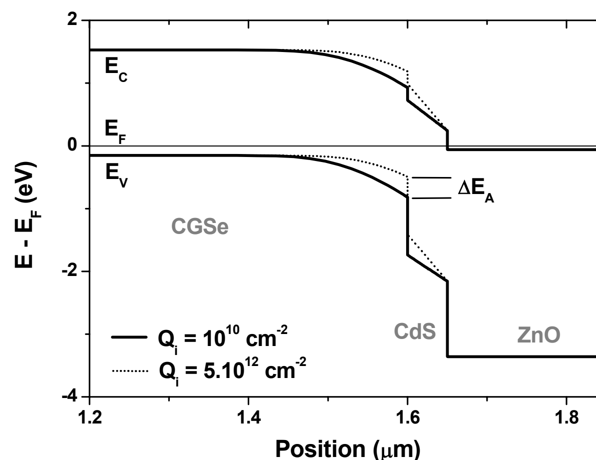

Figure 79. Modification of the band diagram at the CGSe/CdS interface of a typical CGSe-based device for two different densities of occupied acceptor-like states at the junction, 10^{10} cm^{-2} (solid) and $5\cdot10^{12}$ cm^{-2} (dotted line). ΔE_A denotes the net reduction in the potential barrier for holes to activate interface recombination.

In the case of two-stage samples, the temperature dependence of the ideality factor in darkness is comparable to the case under illumination down to temperatures of 230 K, below which departures from the diode-controlled range were found in the corresponding J(V,T) characteristics shown in Figure 76. Values of the ideality factor in darkness for T>230 K are comprised between 1 and 2, in agreement with thermally assisted interface recombination, with tunneling enhancement dominating only at lower temperatures. Higher values of the ideality factor are recorded on the same sample under illumination, indicating that the transition to tunnelling enhancement takes place at higher temperatures compared to the case of measurements in darkness.

Comparable values of E_{00} are found from the fits of the ideality factor as a function of the temperature of single- and two-stage based devices under illumination, as well as similar values of the saturation current activation energy obtained from illuminated J-V curves, leading ultimately to comparable values of the open-circuit voltage. It is thus concluded that two-stage based devices, although capable of improving the collection efficiency of minority carriers by enlarging their effective diffusion length in the absorber film (and consequently improving the short-circuit current density delivered by the cell), present a common limiting factor to the case of single stage processed devices, namely the dominance of interface-mediated recombination. This type of recombination accounts for losses in the obtainable open-circuit voltages, leading to comparable V_{OC} figures recorded from these devices. Additionally, the reduction of leakage currents, via a significant increase of the shunt resistance together with the reduction of the saturation current in two-stage based devices, result in improved values of the fill factor, being related to a reduction of the density of deep defects in the energy band gap associated to the Ga-enrichment stage. The increase of short-circuit currents and the improvement of fill factor figures lead together to higher efficiency values obtained from two-stage based devices, as shown in Table 7, with minor changes in the open-circuit voltages compared to the case of single-stage samples.

Similar limitations are inferred for the case of devices based on Cu-precursors. Although the proposed analysis of the J(V, T) characteristics is not applicable to this type of samples, due to the reduced range of diode-controlled electronic transport in the forward bias range these samples show, extrapolated values of the open-circuit voltage a T=0 K, as shown in Figure 80, are in agreement with interface recombination mechanisms as the dominant process under operating conditions. Furthermore, similar values of the extrapolated open-circuit voltage and the rate of change with the temperature are found compared to those from single and two-stage devices, pointing to a common limiting factor related to the interface quality in all devices processed on CVD-grown CGSe absorbers.

As comparison, high-efficiency CGSe devices from vacuum-based processes are reported to be limited by bulk recombination with reduced tunnelling enhancement[201,198]. Corrected Arrhenius plots of the saturation current from J_{SC}-V_{OC} analysis of solar cells prepared by co-evaporation before and after short annealing in air at 200°C gave activation energies corresponding to the band gap energy, with differences in the tunnelling energy E_{00} attributed to a reduced tunnelling contribution from a decreased charge density in the material upon air annealing. Correspondingly, PVD-based CGSe devices have shown V_{OC} values close to 900 mV, with even higher figures predicted for this high-band gap material[k] if the electronic p-n junction of the device could be displaced from the metallurgical interface (i.e. mismatching the point of highest recombination rate from the point with the highest density of recombination centres).

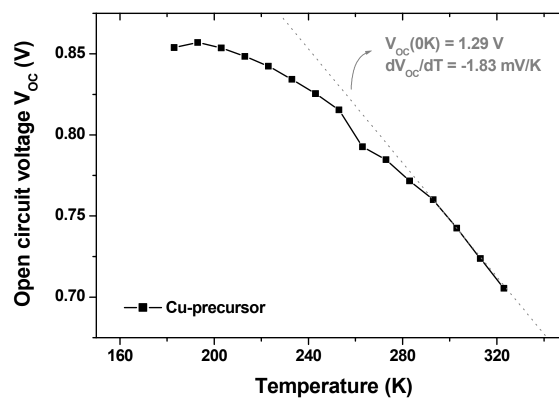

Figure 80. Open-circuit voltage as a function of the temperature of a CGSe-based device processed from a 200 nm thick Cu-precursor following the two-stage recipe, and extrapolated value at T=0 K.

We turn now the attention to the appearance of a blocking behaviour in the J-V curves at low temperatures, recorded as a ‘knee’ readily observable in illuminated J-V curves plotted in linear scale around the values of the open-circuit voltage, as shown in Figure 81 for the case of a two-stage sample. At first glance, this effect seems to be limited to the case of measurements performed under illumination, where an inflection point is inferred at medium forward bias ranges, changing the type of curvature of the

[k] A phenomenological relation[8] between the energy band gap of $CuInSe_2$ and $Cu(In,Ga)Se_2$ and the experimental open-circuit voltage obtained from related devices, in which type inversion is presumed to take place in the near-surface absorber region, reads V_{OC}~E_g/q-500 mV. Thus, V_{OC} values above 1 V could in principle be expected from $CuGaSe_2$-based devices.

corresponding J-V characteristic. Resulting from this bending, the total current flowing through the device approaches zero for $V>V_{OC}$ at low temperatures, a fact that can only be attributed to a non-linear component not included in the single diode model of the equivalent circuit proposed in Chapter 2 for the simulation of the solar cell. Furthermore, the drastic reduction of the output current in the high forward-bias range, which otherwise should be controlled by the exponential bias dependence of the main diode building up the heterojunction, can only be accounted for with a similar component (i.e. a secondary diode) with opposite polarisation to that associated to the main p-n junction.

Such effect has been reported in the literature from a variety of thin-film solar cells, particularly in those based on chalcopyrites[202,203,204] and CdTe[205,206,207] absorber films. The origin of the blocking behaviour is controversial, with two proposed models predicting similar results. Whereas in the case of CdTe solar cells the secondary diode has been systematically attributed to a non-ohmic rear contact of the device, an alternative model including charging and discharging of acceptor-like interface states at the active heterojunction has been reported for chalcopyrite based devices[208,209,210]. Numerical simulations have proven the validity of both approaches for predicting results in good agreement with experimental data, despite of fundamental differences between both models regarding the associated electronic transport. In particular, the active role of near-interface defects in the electronics of the heterojunction should result in observable losses in the open-circuit voltage in devices limited by interface recombination, as discussed above, as long as charging and discharging of interface states is associated to a modification in the potential barrier activating the recombination. The fact that some of the devices reported in the literature showing the blocking behaviour might be limited by bulk recombination, hinders to some extent the analysis of the interface on the basis of electronic characterisation (e.g. by I-V measurements), thus relying on numerical simulations or defect spectroscopy analysis.

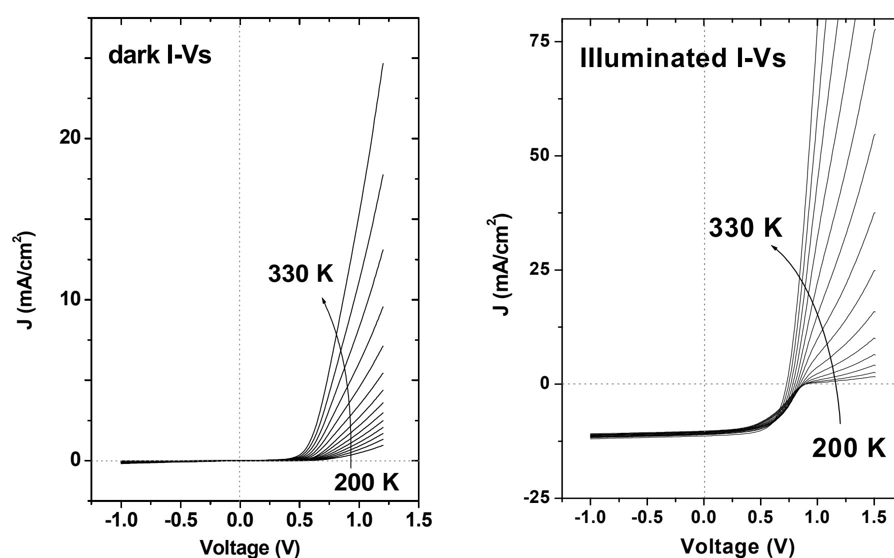

Figure 81. Dark and illuminated J-V curves of a two-stage based CGSe device for various temperatures. A blocking behaviour is inferred from the knee of illuminated I-V characteristics showing up at low temperatures and high forward-bias.

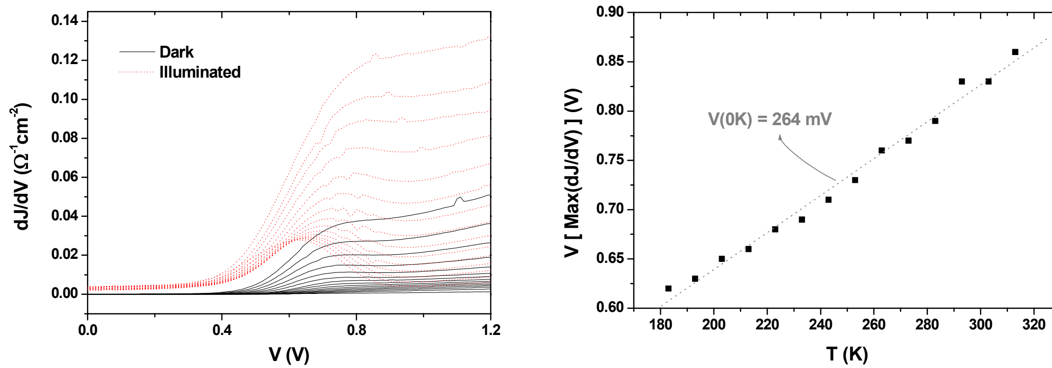

Figure 82. (Left) Derivative of the dark (solid) and illuminated (dotted lines) J-V curves shown in Figure 81 for different temperatures. Maxima in the illuminated J-V curves correspond to inflection points associated to the blocking behaviour. **(Right)** Temperature dependence of the biasing voltage at which the inflection points of the illuminated J-V curves appear, and linear fit with extrapolated value at 0 K.

In the present case, the blocking behaviour is apparently missing in the J-V curves obtained from measurements in darkness, which do not show any inflection point in the forward bias range, as deduced from the derivative of the current density over the applied bias shown in Figure 82 (left), but a significant change in conductance in the same bias range where the inflection shows up in the illuminated J-V curves. However, when bringing together both sets of J-V curves, from dark and illuminated measurements, it turns out that similar total current densities are recorded. Furthermore, both dark and illuminated J-V curves tend to converge at low temperatures for bias $V>V_{OC}$, as can be seen in Figure 83 for pairs of dark and illuminated J-V curves at selected temperatures. This observation leads us to conclude that the effect responsible for the blocking behaviour, clearly visible in those measurements performed under illumination, is actually also recorded in measurements conducted in darkness via a measurable change in conductance, and thus being attributable to an additional element in the equivalent circuit connected in series to the main diode. This observation explains why the single diode model still provides satisfactory results for the fit of dark J-V curves, although the high values of the associated series resistance found in the first part of this section cannot be solely attributed to a linear element of the equivalent circuit.

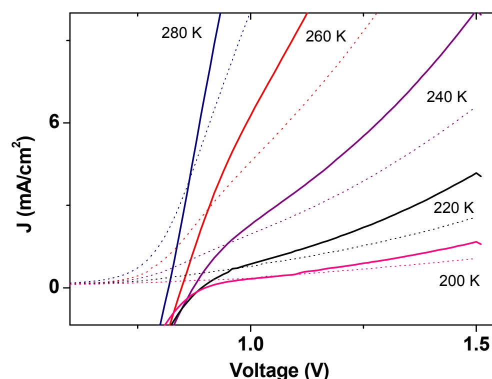

Figure 83. High forward-bias range of dark (dotted) and illuminated (solid) I-V curves from Figure 81 for selected temperatures.

In order to gain some insight into the nature of the blocking behaviour, the fitted values of the series resistance from dark J-V measurements have been monitored as a function of the temperature, as shown in Figure 84 for a pair of samples from single and two-stage based devices. The process behind the apparent series resistance is thermally activated, as concluded from the corresponding Arrhenius plots, with similar activation energies in the range of 260-270 meV for both types of samples. This fact points to a common origin of the blocking behaviour, independently of the type of process followed for the absorber deposition, with high values of the apparent series resistance found in both single- and two-stage based devices, as discussed above. Such high values of the thermal activation of the associated series resistance are far too high to be related to potential barriers at grain boundaries, which might inhibit the electronic transport at low temperatures, as will be shown in the next Chapter on the basis of KPFM studies on the rear side of the absorber layer over CGSe grain boundaries. Thus, an alternative potential barrier for injected majority carriers (i.e. holes), amounting for ~300 meV in order to account for the observed activation energies of the associated series resistance, must be included in the band diagram of these devices.

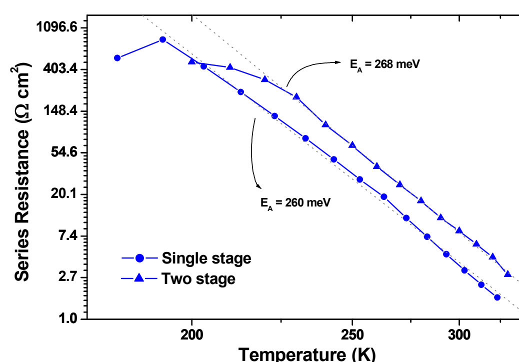

Figure 84. Series resistance obtained from single diode fits of dark J(V,T) curves as a function of the temperature of a pair of devices based on single- and two-stage grown CGSe absorbers and corresponding activation energies.

A further hint of the common nature of the observed blocking behaviour under illumination and the change in conductance recorded in darkness is shown in Figure 82 (right), where voltages corresponding to the appearance of the inflection point (obtained from the maxima in the corresponding dJ/dV vs. V plots) of illuminated J-V curves are plotted over the temperature. Extrapolating the linear fit to T=0 K, a voltage of 264 mV is obtained, in good agreement with the activation energy of the associated series resistance from dark measurements. Remarkably, the blocking behaviour, though being more evident in illuminated J-V curves, does not seem affect the PV parameters (in particular values of the open-circuit voltage), as concluded from the inspection of J_{SC}-V_{OC} plots shown in Figure 76 for the case of single- and two-stage based devices, thus allowing the I(V,T) analysis proposed in Chapter 2 and discussed above.

A model accounting for the blocking behaviour observed in the J-V curves of these samples is proposed in Figure 85. Contrarily to the case of reported theories of non-ohmic Mo/chalcopyrite contacts, and basing on the experimental observations from

Chapter 3 on the presence of an interfacial $MoSe_2$ layer mediating the rear contact of CVD-based devices, it is proposed that the potential barrier for the hole transport under forward bias results from a valence band offset between the $MoSe_2$ and the CGSe films of nearly 0.3 eV. Such a model accounts satisfactorily for the observed features of the electronic transport at low temperatures, predicting the convergence of dark and illuminated J-V curves to common values of the total current under voltage bias $V>V_{OC}$. Under these conditions, the current of injected holes from the contact into the absorber overcomes the delivered photocurrent in the opposite direction, which is the distinct feature of illuminated J-V curves. The open-circuit voltage corresponds to the bias condition in which the photocurrent is compensated by the injected current (thus J=0), and for any value $V<V_{OC}$ of the applied bias, the photocurrent dominates the hole transport. The potential barrier as depicted in Figure 85 acts thus as a barrier for the injected current and does not affect the value of the open-circuit voltage, which remains controlled by the main diode.

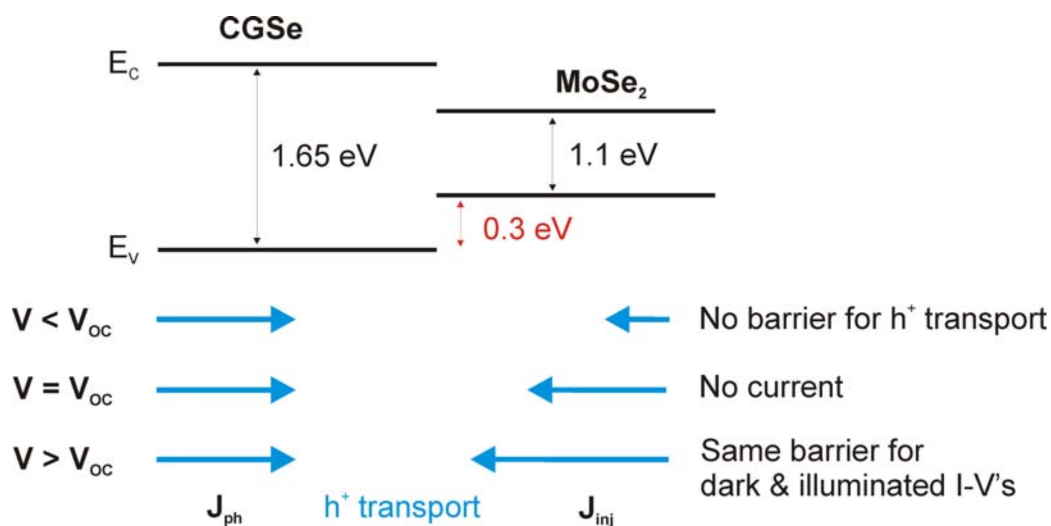

Figure 85. Proposed band diagram of the $CGSe/MoSe_2$ interface at the rear contact and scheme of the hole transport resulting from the contributions of the photocurrent (assumed to be bias-independent) and the injected current for different biasing conditions.

Simulations have been carried out with the help of the software package SCAPS [(200] in order to check the validity of the proposed model. In Figure 86, the performance of a typical CGSe-based solar cell (material parameters are given in Appendix II) with an ohmic rear contact is compared to that recorded from a device with the rear contact mediated by an interfacial p-type $MoSe_2$ layer, including a $CGSe/MoSe_2$ valence band offset of 0.3 eV, as depicted in the band diagrams shown in the insets. Simulated J-V curves for different temperatures qualitatively reproduce the blocking behaviour found in the experiments when including the valence band offset, thus supporting the proposed model sketched in Figure 85.

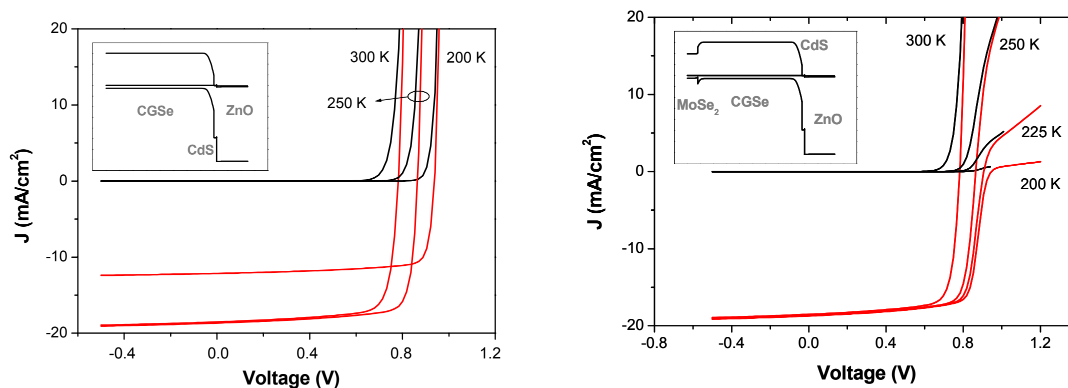

Figure 86. Simulated J-V curves in darkness and under AM1.5G illumination conditions at different temperatures for the cases of a CGSe-based device with an ohmic rear contact **(left)** and that including an interfacial $MoSe_2$ layer with an associated valence band offset of 0.3 eV **(right)**.

4.4 Chapter summary

Results of the electronic characterisation carried out on thin-film solar cells based on CVD-grown CGSe absorbers have been presented in this chapter, complementing the structural study of the heterostructures introduced in Chapter 3.

Interfacial issues, particularly those involving the active absorber layer, as a key element of heterojunction-based devices, have deserved special attention. The study of the p-n junction in state-of-the-art CVD-grown CGSe devices, between a two-stage grown CGSe film and the CdS buffer layer, has been carried out by means of photoelectron spectroscopy, leading to estimations of the valence (-1.0±0.2 eV) and conduction band (-0.25 eV>ΔE_C>-0.60 eV) offsets at the interface. In agreement with results reported in the literature, and supported by TEM analysis, evidences of a disordered phase in the near-surface region of two-stage-grown CGSe absorbers have been presented. This surface phase has been related to a distinct bias dependence of the quantum efficiency of complete devices, when comparing to the results obtained from single-stage based samples, presumably due to Fermi level pinning at the highly defected interface.

The electronic characterisation, performed by means of quantum efficiency, EBIC and current-voltage analysis, has been carried out with the aim of assessing the performance of devices processed from the modified absorber growth approaches introduced in Chapter 3. Results of a comparative study including single stage, two-stage and Cu-precursor-based devices have been presented. It has been found that devices based on Cu-precursors are affected by low values of the shunt resistance, and consequently by poor fill factors resulting from a limited bias-range of diode-controlled transport. Improved PV performance has been demonstrated from devices based on two-stage grown absorbers, with top efficiencies of 7.2 % under standard AM1.5G illumination conditions. Quantum efficiency, EBIC and current-voltage characteristics have revealed that the improvement recorded in the performance of two-stage samples is due to higher fill factor and short-circuit current figures, resulting from the reduction of leakage

currents and the enlargement of the effective diffusion length of minority carriers in the absorber film, compared to the reference case of single-stage based devices. Limitations of the obtainable open-circuit voltage have been found to be related to the active role played by the CGSe/CdS p-n junction in the device electronics, controlling the electronic transport via interface recombination of charge carriers. This issue constitutes a fundamental limiting factor of all CGSe-based devices studied in this work.

Finally, the appearance of a blocking behaviour in the current-voltage characteristics of CGSe-based devices at low temperatures has been identified as responsible of the significantly high values of the apparent series resistance obtained from single diode fittings of J-V characteristics. This effect has indeed been related to the $MoSe_2$ interfacial layer at the rear contact reported in Chapter 3. A band diagram of the CGSe/$MoSe_2$ interface has been proposed, accounting for the observed effects of current blocking. Numerical simulations have been carried out, supporting the validity of the model.