

Amorphous Gallium-Oxide-Based Non-Filamentary Memristive Device with Highly Repeatable Multiple Resistance States

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A memristive device is presented based on a Ti/GaO_x/W stack with an amorphous GaO_x layer deposited at a low temperature (250 °C) using plasma-enhanced atomic layer deposition. The device fabrication is compatible with a standard complementary metal oxide semiconductor back-end-of-line technology. The area dependence of the resistance values for both high and low resistance states indicates that switching takes place over the entire device area via a non-filamentary-based mechanism. Evidence is provided that the switching process originates from a field-driven oxygen exchange between the interfacial TiO_x layer and the GaO_x one as well as from the charging/discharging of interfacial trap states. The devices reveal self-rectifying characteristics with high cycle-to-cycle reproducibility. Multiple states can be programmed with 12 distinct intermediate states during potentiation, and 11 distinct states during depression. This amorphous GaO_x-based memristive device with highly reproducible multi-level resistance states shows great potential for enabling artificial synapses in neuromorphic applications.

1. Introduction

There is a growing interest in memristive devices due to their potential to build neuromorphic computing systems based on their ability to mimic biological neurons and synaptic behaviors.^[1] In particular, memristive devices can be electrically programmed to exhibit multi-level resistance states, which is one of the important requirements for constructing electronic neural networks.^[1–3] There are different types of memristive devices relying on different mechanisms.^[4] One of the widely studied concepts is the voltage-driven migration of oxygen ions and subsequent valence change within a spatially confined filamentary region, known as a filamentary valence change memory (VCM).^[5,6] However, those systems usually suffer from device-to-device and cycle-to-cycle variability due to their stochastic nature,^[6] and from a lack of

multi-level operation. In addition, their typical high-operation currents represent one of the major challenges for the integration of filamentary-type switching devices in neuromorphic circuits.^[7]

In contrast, area-dependent switching systems suffer less from stochasticity and offer high cycle-to-cycle reproducibility with multiple intermediate states, enabling a predictable weight update, which is crucial for neuromorphic computing.^[6–8] Filament forming does not occur in area-dependent switching systems. Instead, the resistance levels scale with the electrode area suggesting that switching takes place homogeneously over the entire interface.^[8–10] The electrode area can be scaled down to attain low operation current levels needed for low power operation, which makes integration in neuromorphic circuits considerably easier. Interface-type switching devices also provide a self-rectifying mechanism and allow selector-less operation.^[11]

Perovskite oxides like Pr_{0.3}Ca_{0.7}MnO₃ (PCMO),^[8,12–15] and SrTiO₃ (STO)^[16] have played a significant role in elucidating the mechanisms underlying non-filamentary interface type switching. These mechanisms primarily involve interfacial redox reactions driven by the drift and exchange of oxygen vacancies at the electrode/oxide interface. Similarly, TiO₂,^[17,18] and Ta₂O₅^[19] have been extensively studied, where oxygen vacancy dynamics modulate the contact resistance, resulting in resistive

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switching. In addition to oxygen vacancy exchange, trapping and de-trapping of charge carriers within the insulating layer or at the metal/insulator interface have also been proposed, particularly in PCMO,^[20] STO^[21–23] and Nb₂O₅^[24,25] systems where charge carrier dynamics influence the conduction and carrier injection at the interface.

Among resistive switching oxides, GaO_x has emerged as a promising candidate for non-filamentary bulk switching due to its mixed ionic-electronic conduction properties. Aoki et al. demonstrated non-filamentary bulk memristive switching in pulsed laser deposited (PLD) sub-stoichiometric amorphous GaO_x thin films.^[26] Their work revealed that resistive switching is associated with the bulk motion of ions, as evidenced by photoemission and transmission electron microscopy (TEM). Similar characteristics have been reported – also in PLD deposited amorphous GaO_x layers – suggesting that introducing oxygen vacancies in a-GaO_x and manipulating their movement is key for resistive switching.^[27–30] Moreover, it has the potential, as other semiconducting oxides to be back-end-of-line (BEOL) compatible for the integration of devices on top of complementary metal oxide semiconductor (CMOS) chips. In most studies on a-GaO_x memristive devices reported so far, PLD was used for the growth of the sub-stoichiometric films. PLD, however, is not desirable for CMOS technology as it is not easily scalable. Memristive devices were demonstrated using amorphous chromium-doped GaO_x thin films deposited by co-sputtering of Ga₂O₃ and Cr targets at room temperature.^[31] Very recently, W/WO_x/a-GaO_x/ITO synaptic devices were reported and rf sputtering was used for the deposition at ambient temperature of a-GaO_x.^[32] BEOL-compatible memristive devices based on a-GaO_x grown by ALD still need to be addressed.

In this paper, we demonstrate a Ti/a-GaO_x/W memristive device with an amorphous sub-stoichiometric GaO_x layer deposited at 250 °C using plasma-enhanced atomic layer deposition (PE-ALD). The stack offers excellent integrability in the CMOS BEOL due to the low-temperature PE-ALD process. A GaO_x layer is deposited on Ti resulting in the formation of an interfacial TiO_x layer between GaO_x and Ti, which significantly influences the switching behavior. To gain a deeper understanding of the role of this interfacial oxide, two additional stacks are studied: TiN/GaO_x/W with TiN being the reactive metal to form an intermediate TiO_xN_y layer and Pt/GaO_x/W with Pt being a noble metal to avoid the formation of an interfacial oxide. We achieve Ti/a-GaO_x/W devices with highly reproducible multi-level resistance states under identical pulses enabling their use as artificial synapses. We also show that the device operation current can be engineered simply by controlling the oxygen content in GaO_x by varying the O₂ plasma exposure time during PE-ALD deposition.

2. Results and Discussion

2.1. Device Structure and Composition

In an earlier work, we demonstrated the tuning of non-stoichiometric a-GaO_x layer conductivity by varying the O₂ plasma exposure time during PE-ALD.^[33] The lower the O₂ plasma time is, the higher the oxygen vacancy concentration is, eventually leading to a semiconducting behavior.^[33] We recently demonstrated a 3-terminal field-effect-based charge trap mem-

ristive device based on amorphous semiconducting GaO_x.^[34] For an O₂ plasma time of 15 s or more, the films are insulating. The signature of oxygen vacancies is evidenced by spectroscopic ellipsometry for O₂ plasma time of 8 s or less. This is illustrated in Figure S1 (Supporting Information). The extinction coefficient, plotted as a function of energy, is independent of the O₂ plasma exposure time in the energy range corresponding to the bandgap (Figure S1a, Supporting Information). In the sub-bandgap range, two absorption peaks are observed for 8 s O₂ plasma time (Figure S1b, Supporting Information). These peaks can be attributed to oxygen vacancy states, predicted by DFT calculations to be located at ≈2.75 and 3.6 eV and likely to form in under-oxidized GaO_x.^[35–37] For 1 s O₂ plasma time, the two peaks turn into a broad intense peak, consistent with a larger amount of oxygen vacancies in an amorphous film (with a large distribution of interatomic distances). In contrast, the absence of such peaks for the 15 s plasma time suggests a near-stoichiometric composition. While the oxygen stoichiometry is challenging to measure in thin films, spectroscopic ellipsometry measurements clearly show the increase of oxygen vacancies with decreasing O₂ plasma times resulting in localized defect states that primarily influence sub-bandgap absorption without significantly altering the intrinsic bandgap. A similar behavior has been observed in PLD-deposited oxygen-deficient a-GaO_x films reported by Kim et al.^[38]

In this study, we focus on a-GaO_x films grown using 8 s O₂ plasma time. The schematic illustration of the investigated two-terminal Ti/GaO_x/W memristive device is presented in Figure 1a. The stack is deposited on a p++-type Si substrate with 300 nm thermal oxide. It consists of a sputtered 60 nm W/40 nm Ti bottom electrode, a 30 nm GaO_x film deposited at 250 °C by PE-ALD using 8 s O₂ plasma time and a sputtered 60 nm W layer for the top electrode. Devices with various areas ranging from 30 × 30 μm² to 100 × 100 μm² were patterned on the sample using direct laser writing lithography. Figure 1b shows a cross-section of a device obtained using scanning transmission electron microscopy (STEM). The image shows a GaO_x uniform layer of 30 nm thickness. An interfacial layer with different contrast is also observed between GaO_x and the bottom Ti layers. The measurements by energy dispersive X-ray spectrometry (EDX), shown in Figure 1c, reveal the existence of a TiO_x interfacial layer of ≈7 nm thickness (colored dark blue) between the GaO_x and Ti interfaces. It originates from the strong oxidizing conditions for Ti during the O₂ PE-ALD deposition of GaO_x on Ti. During the first ALD cycles, the Ti bottom layer is indeed exposed to 8 s-time periods of O₂ plasma. While the O₂ plasma is essential for reacting with the gallium precursor adsorbed on the surface (thermal ALD with trimethylgallium does not work) and is not sufficient to fully oxidize it, it also oxidizes the Ti bottom electrode, resulting in the observed interfacial TiO_x layer. The influence of this TiO_x interface oxide on device characteristics and performance will be discussed in the following sections.

2.2. Resistive Switching

Figure 2a shows the typical *I*–*V* characteristics of a Ti/GaO_x/W memristive device (100×100 μm² area). It exhibits a bipolar hysteretic behavior. A positive voltage of 8 V is applied to the top electrode (W) to set the device from a high resistive state (HRS) to a

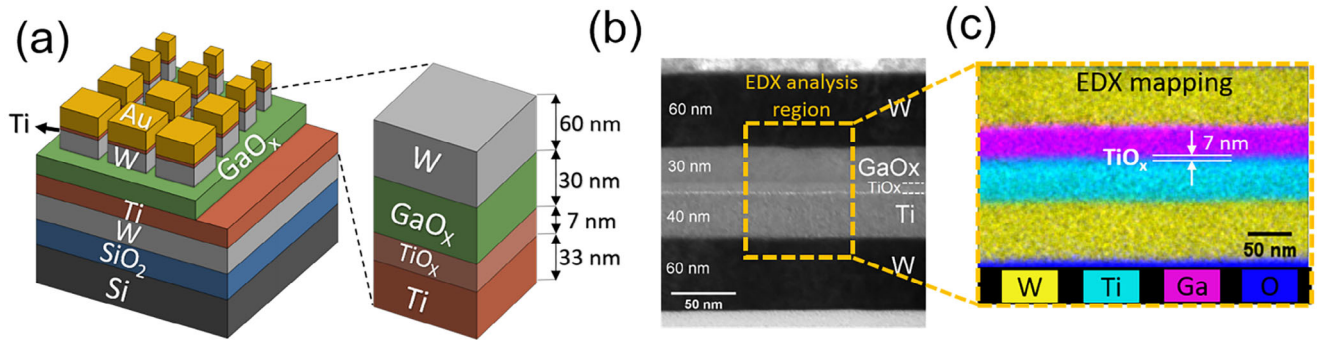


Figure 1. a) Sketch of the 60 nm W/40 nm Ti/30 nm a-GaO_x/60 nm W stack deposited on 300 nm SiO₂/Si substrate. The top W electrode is capped with 10 nm Ti/100 nm Au). b) Cross-sectional STEM image of the stack. c) Elemental map obtained from EDX indicates the presence of a ≈7 nm TiO_x interfacial layer between a-GaO_x and Ti (bottom electrode).

low resistance state (LRS). Using a negative voltage of -1.5 V on the top electrode, the device is resets back to HRS. At a 4 V read voltage, the ON current (I_{on}) is ≈ 160 nA and the OFF current (I_{off}) is ≈ 50 nA for the LRS and HRS, respectively. These devices reveal self-compliance switching characteristics and do not require any forming step to initiate the device functionality. Hence the device can allow selector-less operation. Similar characteristics have been reported for area dependent switching cells,^[8–10] including GaO_x devices,^[26] where switching takes place across the entire area, suggesting a homogeneous, non-filamentary switching system. Another supporting indication for homogeneous switching is that our device shows a non-abrupt but gradual resistance change during voltage sweep, unlike the filamentary ones.^[4,17] In Figure 2b we show the I – V characteristics of devices with electrode areas ranging from 30×30 to $100 \times 100 \mu\text{m}^2$ for a positive voltage sweep. The area dependence of the resistance values for both HRS and LRS at 4 V read voltage is given in the inset. We observe a linear dependence of device resistance with area while the memory window remains the same. This observation strongly suggests that the switching phenomenon occurs across the entire electrode area, rather than being confined to a filament.

To confirm the role of the Ti bottom electrode and its interfacial oxide on the switching mechanism, two additional stacks with TiN and Pt bottom electrodes were investigated. The I – V characteristics of Ti/GaO_x/W, TiN/GaO_x/W, and Pt/GaO_x/W devices are presented in Figure 3a,b, and c respectively. At positive bias, Pt/GaO_x/W exhibits almost no hysteresis. The small hysteresis observed below 4 V is volatile, i.e., for each consecutive positive voltage sweep the device starts back from HRS (shown in the Figure S2, Supporting Information). This hysteresis is likely due to charge trapping in the GaO_x layer or at its interfaces. The devices with TiN exhibit the largest memory window and can sustain the largest voltage (up to 10.5 V here). However, we observe large cycle-to-cycle variations in this stack (see Figure S3, Supporting Information). The devices with Ti show stable and repeatable Set/Reset cycles.

The switching properties thus highly depend on the electrode material. Both Ti and TiN electrodes result in the formation of an interfacial oxide in the presence of oxygen.^[39,40] The conditions are particularly oxidizing for the bottom electrode in the first cycles of the PE-ALD growth of GaO_x due to O₂ plasma exposure. Pt is much less prone to oxidize.^[39] Therefore, the hysteresis ob-

served for devices with Ti and TiN bottom electrodes originates from the active role of the interfacial layer (TiO_x or TiO_xN_y) in the switching mechanism. Let us focus now on the devices with Ti bottom electrodes to discuss the switching mechanism.

We propose that the resistive switching depends on the oxygen exchange between GaO_x and TiO_x.

Let us first analyze the transport processes involved in both HRS and LRS. We considered different models to fit the I – V data in the different voltage regimes (different slopes): thermionic emission (TE), trap-assisted tunneling (TAT), Fowler–Nordheim tunneling (FN), and Poole–Frenkel (PF) emission models. Among these, the TAT model for the low voltage regime (2.0–4.0 V for HRS and 1.8–3.8 V LRS) and the PF emission for the high voltage regime (4.0–7.2 V in HRS and 3.8–6.6 V in LRS) provide the best fits to the data.

A generalized TAT model is given by Houngh et al.^[41]

$$J_{TAT} \propto \exp\left(-\frac{8\pi\sqrt{2qm_{ox}}}{3h}\Phi_t^{3/2}\frac{1}{E}\right) \quad (1)$$

where h is Planck's constant, Φ_t is the energy of the traps below the oxide conduction band, m_{ox} is the effective electron mass in the oxide and E is the electric field. The linear fitting shows excellent agreement with the measured I – V data, with R^2 values close to 1 for both the HRS (0.998) and LRS (0.997) as shown in Figure 4a. The slope of the plot $\ln(J)$ versus $(1/E)$ was used to extract the trap state energy. The calculated trap energies Φ_t are 0.32 and 0.24 eV for HRS and LRS respectively. This change in trap energy levels between HRS and LRS is attributed to changes in the oxygen vacancy concentration, which increases the availability of trap states for electron conduction.

In the higher voltage regime, the conduction mechanism is well described by Poole–Frenkel (PF) emission, which is expressed by the following relation:

$$J_{PF} = q\mu N_0 E \exp\left(\frac{-q}{k_B T}\left(\Phi_D - \sqrt{\frac{qE}{\pi\epsilon}}\right)\right) \quad (2)$$

where J_{PF} is the current density, E is the electric field, N_0 is the defect concentration, Φ_D is the defect trap energy, and ϵ_r is the relative dielectric constant. A linear fit for $\ln(J/E)$ versus $E^{1/2}$

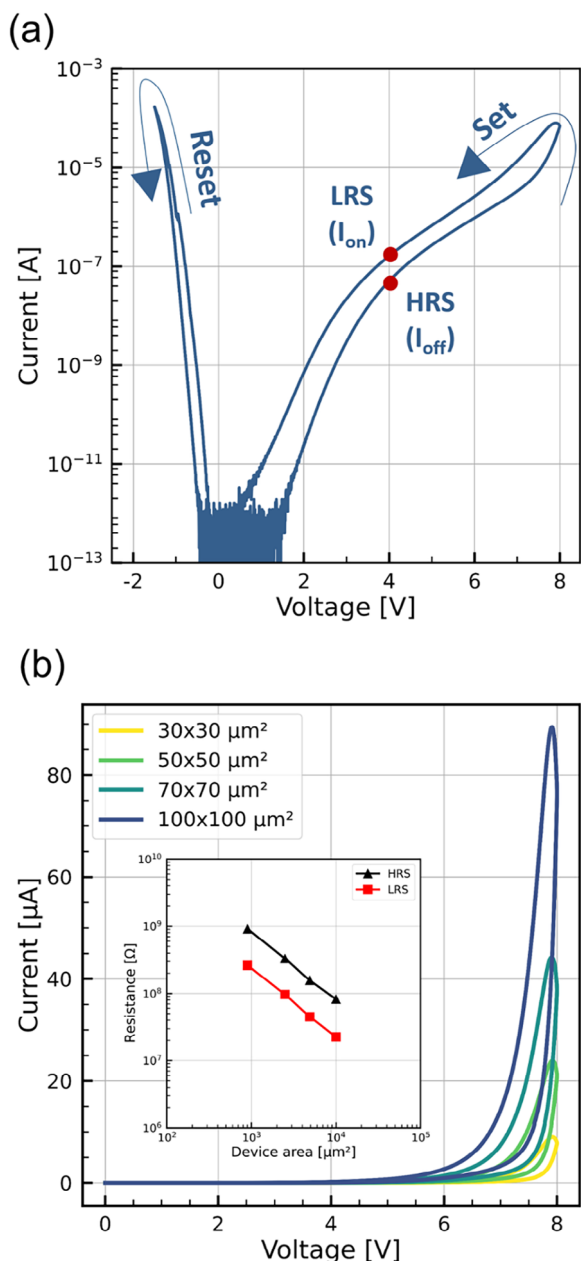


Figure 2. Current-voltage characteristics of a Ti/GaO_x/W device. a) *I*–*V* curve of a device with 100 × 100 μm² area showing a hysteresis behavior. To set the device, the voltage is swept to +8 V and to reset, it is swept to –1.5 V. Arrows indicate the sweep direction for set and reset operations. b) *I*–*V* characteristics for devices with different areas. The inset shows HRS and LRS resistance values at 4 V read bias. The linear dependence of the resistance as a function of area confirms the non-filamentary conduction.

(Figure 4b) is obtained with R^2 values 0.998 and 0.997 for HRS and LRS respectively. The extracted value for ϵ_r is found to be 9.9 for both HRS and LRS, which aligns very well with the dielectric constant of 9.8 reported in our previous work.^[33] The defect trap energy Φ_D for HRS is found to be 0.72 eV. A similar value (0.70 eV) has been reported for P–F emission in β -Ga₂O₃.^[42] In LRS, the defect energy slightly decreases to 0.69 eV. The accu-

mulation of oxygen vacancies near the TiO_x/GaO_x interface may contribute to reducing the effective barrier height. To summarize, both in HRS and LRS, the transport at “low” voltage is dominated by TAT and at “high” voltage by P–F.

With this analysis, the band diagram shown in Figure 4c is proposed for the TiO_x/GaO_x device. Ti exhibits a work function of 4.33 eV.^[43] The electron affinity of amorphous TiO_x is of ≈3.8 eV.^[44] Due to the strong oxidizing conditions experienced by Ti during the O₂ plasma growth of GaO_x, TiO_x is considered rather insulating (and not semiconducting).

The electron affinity of stoichiometric crystalline β -Ga₂O₃ has been reported in the range of 3.5–4.0 eV.^[45,46] Additionally, a study on Sn-doped amorphous Ga₂O₃ reported an electron affinity of ≈4.0 eV.^[47] For this study, we assumed an electron affinity of 3.5 eV for GaO_x. The oxygen vacancies in GaO_x introduce defect states below the conduction band (depicted as red lines in Figure 4c).

Now let’s consider the switching from HRS to LRS. When the applied voltage is increased beyond 7 V up to 8 V, the current increases strongly (change of slope in the *I*–*V* curves), and the device is set to the LRS. When a positive bias is applied to the top W electrode, the positively charged oxygen vacancies (V_o⁺) from the GaO_x film migrate toward TiO_x and accumulate in TiO_x and near the TiO_x/GaO_x interface (top panel of Figure 4d). This increased density of defects and associated traps leads to an increased current flowing through the TiO_x/GaO_x interface and the TiO_x layer by trap-assisted electron tunneling. This is consistent with the decrease of the average trap barrier from 0.32 eV in HRS down to 0.24 eV in LRS. The high density of oxygen vacancies in TiO_x may also contribute to other transport mechanisms across TiO_x, leading to enhanced conduction through the whole stack. Conversely, applying a negative voltage to the top electrode causes the oxygen vacancies to be pushed back from TiO_x into the bulk of GaO_x (bottom panel of Figure 4d). This redistribution of oxygen vacancies reduces the density of trap states available for electron conduction in the TiO_x layer. Consequently, the device switches back to the HRS.

Thus, the TiO_x barrier contributes to the change in overall cell resistance by field driven exchange of oxygen vacancies while the GaO_x layer serves as a reservoir of oxygen vacancies. This is similar to the tunnel barrier-based resistive RAM (ReRAM) concept, where the switching mechanism is explained by the exchange of oxygen between a conductive metal oxide and the tunnel oxide layer.^[48] A similar interface-type switching mechanism has been reported in PCMO, one of the most intensively studied oxide for interfacial switching, with different reactive electrodes such as Ti, Ta, and TiN.^[13–15]

To further investigate the impact of oxygen vacancies and their concentration, a sample was prepared with a GaO_x layer deposited by using a shorter O₂ plasma exposure time of 1 s, resulting in a much larger oxygen vacancy content (see Figure S1, Supporting Information). These devices exhibit three orders of magnitude higher currents at 4 V (Set voltage of 8 V for both) than for the devices prepared with 8 s O₂ plasma time for GaO_x (see Figure S4, Supporting Information), which highlights the role of oxygen vacancies in the GaO_x film for these devices. As expected, the stack with the lower O₂ plasma time during PE-ALD of GaO_x also has a thinner TiO_x layer (≈5 nm) at its interface, as observed by TEM (see Figure S5, Supporting Information), which also

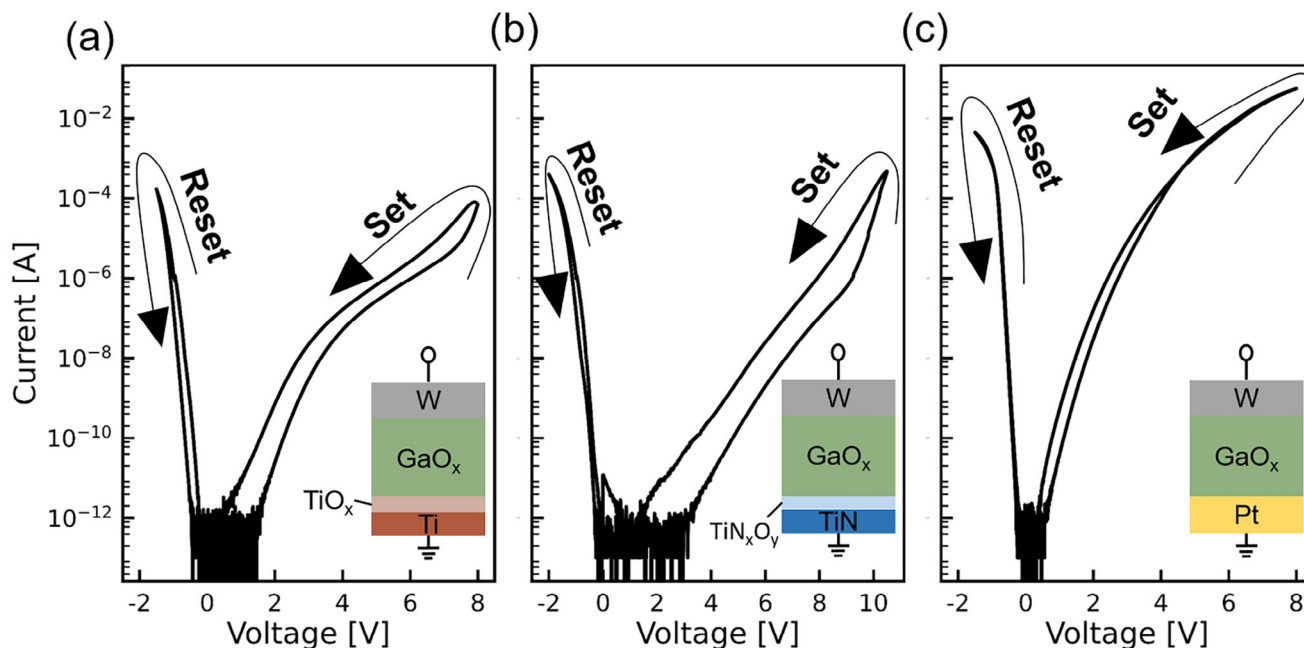


Figure 3. Current-Voltage characteristics of a) Ti/GaO_x/W stack with TiO_x interface layer, b) TiN/GaO_x/W stack with TiN_xO_y interface layer, and c) Pt/GaO_x/W stack without any interface layer. The insets show the cross-sectional schematic corresponding to each stack.

contributes to an enhanced current. This observation has potential implications for further device engineering, as the current levels can be tuned by simply changing the O₂ plasma time during the PE-ALD deposition process.

2.3. Multiple Resistive States

The development of neuromorphic and analog computing requires the memristive device to exhibit several well-defined distinguishable resistance states.

We investigated read currents under various Set/Reset pulse amplitudes and widths. Devices (100 × 100 μm²) were first initialized to HRS (the current measured is 50 nA at 4 V read voltage). Next, a matrix of positive Set voltage pulses of variable pulse amplitudes and widths was applied. The current measured at 4 V read pulses after the application of each Set pulse are presented in **Figure 5a** in a color map. The current level increases with voltage amplitude and pulse width. For lower pulse amplitudes and shorter pulse widths, only a small deviation is observed from the initial HRS (the dark blue color corresponds to the low current range of hundreds of nA). If the pulse width is reduced to obtain faster switching, the Set pulse amplitude needs to be increased in order to reach the same LRS state. For a 9.6 V pulse amplitude it is sufficient to apply a 1 ms pulse while it requires 50 ms pulse width for an 8.0 V amplitude to reach the same current level. The color map indicates a clear trade-off between pulse amplitude and pulse width. Based on these measurements, we have considered in the following an 8 V pulse amplitude with 30 ms pulse width as a Set pulse for our multiple resistance state study.

Having well-defined resistance states is greatly advantageous. However, to be practically useful, it is essential that these

states are both easily distinguishable and repeatable. Potentiation/depression measurements were performed, using the pulse scheme shown in **Figure 5b**. A series of twenty consecutive identical Set pulses (8 V, 30 ms width) were applied to induce potentiation. Following the potentiation phase, fifteen Reset pulses were applied for depression with progressively increasing voltage magnitude to achieve clearly separate resistance states (starting with a pulse of −100 mV and increased by steps of 100 mV, constant pulse width of 5 ms). The current states were read using a read pulse of 4 V and 1 ms pulse width. The whole potentiation and depression sequence was iterated a hundred times. **Figure 5c** shows the gradual modulation of current states for the first three potentiation/depression cycles showing a nearly linear weight update. The current level ranges from 50 to 700 nA, resulting in an ON/OFF ratio of ≈14. The cumulative distributions of potentiation and depression states for the 100 cycles are shown in **Figure 5d**. We demonstrate remarkably narrow distributions for most states with twenty distinct states during potentiation and fifteen distinct states during depression. The stack has an excellent reproducibility of the intermediate states (relative dispersion of resistance less than 2%). Unlike the potentiation process, a linear depression could not be realized using an identical pulse sequence, reflecting an asymmetry between these two processes. This is likely due to the drift and diffusion dynamics of oxygen ions. Differences in energy barriers for ion migration during the accumulation (potentiation) and depletion (depression) of oxygen vacancies (toward or away from the TiO_x interfacial layer) could result in an asymmetrical behavior. Similar asymmetries have been reported and discussed on other systems.^[49,50] To address these challenges, various strategies, including the use of different programming schemes, have been suggested.^[51] In our study, we employed progressively increasing pulse amplitudes during the depression process to reduce the effects of such

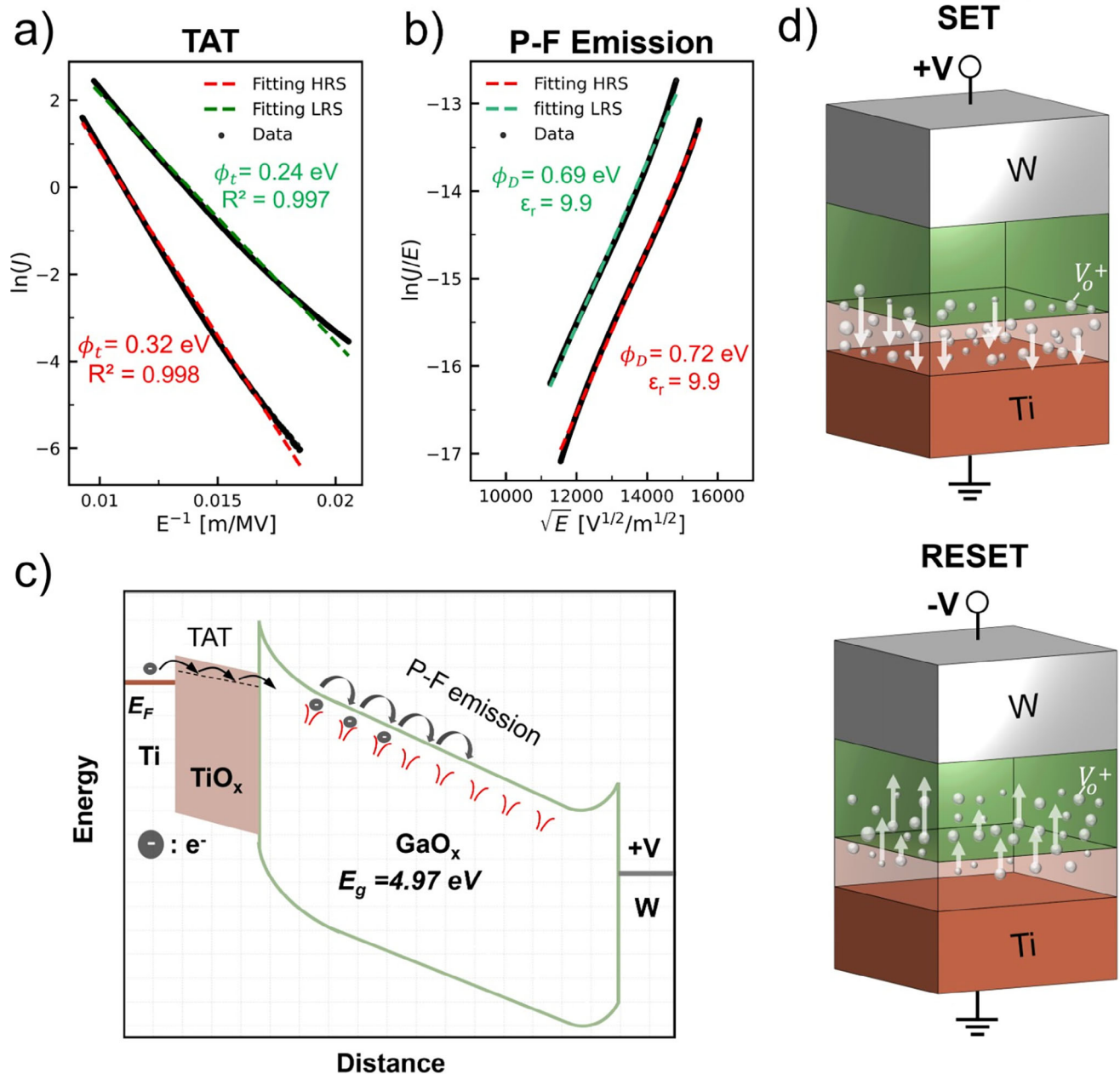


Figure 4. Transport mechanisms and resistive switching mechanisms. a) I - V curves and their fittings using trap-assisted tunneling (TAT) (Equation 1) in the low-voltage regime (2.0–4.0 V for HRS and 1.8–3.8 V for LRS). The green and red dashed lines represent the fits for LRS and HRS, respectively. b) I - V curves and their fittings using the Poole–Frenkel model (Equation 2) in the high-voltage regime (4.0–7.2 V for HRS and 3.8–6.6 V for LRS). The green and red dashed lines represent the fits for LRS and HRS, respectively. c) Schematic representation of the band diagram under positive bias illustrating the two primary conduction mechanisms for both HRS and LRS. In the interfacial 7 nm-thick TiO_x layer, TAT dominates, as electrons tunnel through trap states (dashed line). In the 20 nm-thick GaO_x layer, P–F emission governs the electronic transport. The electrons are emitted from trap states (red lines) to the conduction band. d) Sketches illustrating the oxygen vacancy movement between GaO_x and TiO_x layers during Set (LRS to HRS) and Reset (HRS to LRS) operations. During the Set process ($V > 7 \text{ V}$), oxygen vacancies accumulate in TiO_x and near the $\text{TiO}_x/\text{GaO}_x$ interface, leading to the LRS. In the Reset process, oxygen vacancies migrate away from the TiO_x layer toward GaO_x , restoring the HRS.

asymmetries. However, achieving complete symmetry between potentiation and depression remains a challenge.

Figure 6a shows that the device can withstand 10^3 potentiation and depression operations without failure. From the cumulative statistics over 1000 cycles, we observe more pronounced degradation in lower current states leading to a reduction in the

memory window from ≈ 14 to ≈ 9 . In the potentiation cycles, the dispersion increases, notably at lower current levels (states at current levels below 300 nA), with a relative dispersion of up to 14%. Meanwhile, the narrow distribution is preserved for higher current states ($> 300 \text{ nA}$) with less than 2% relative dispersion, showing high stability. A similar narrow distribution over cycling is

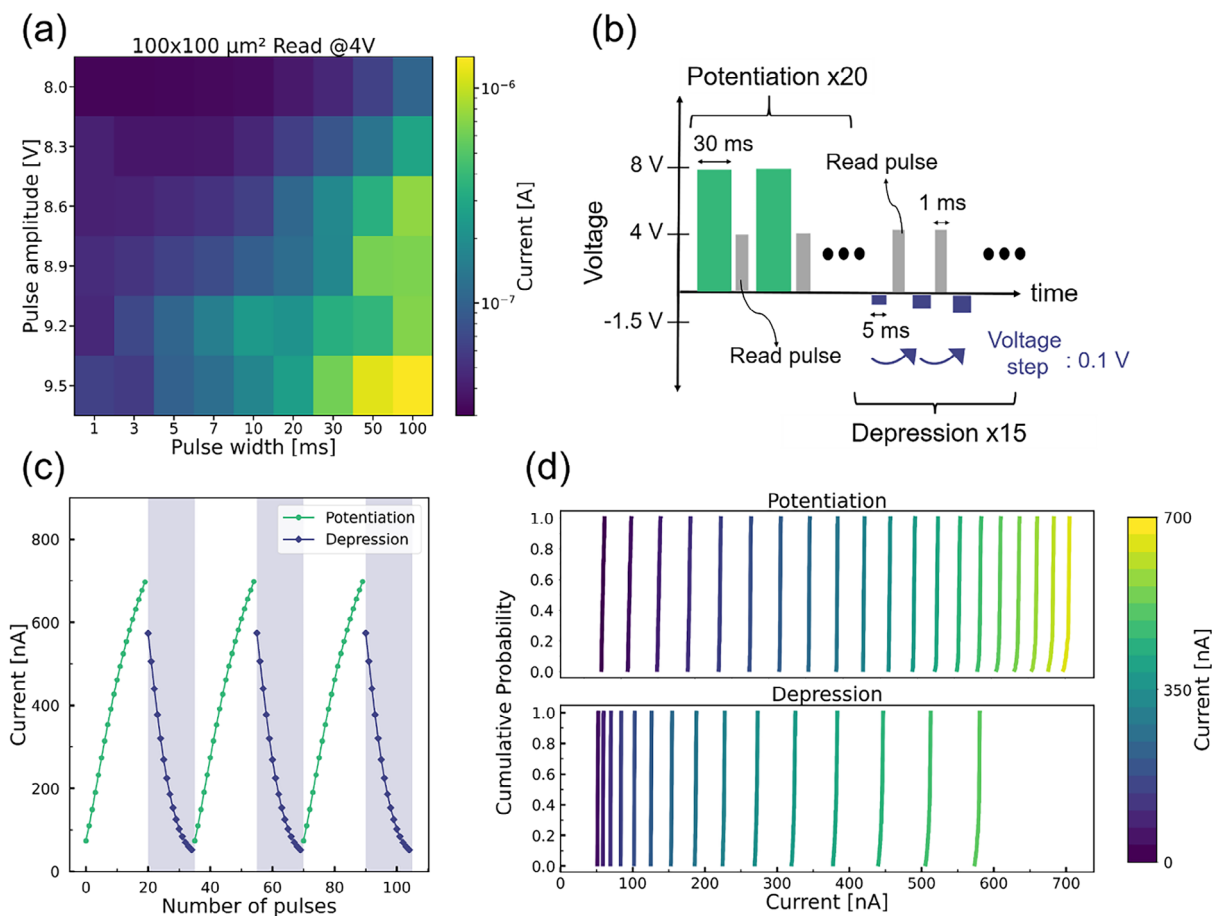


Figure 5. Analog behavior of a Ti/a-GaO_x/W device (100 × 100 μm²). a) Color map showing the current values after positive Set voltage pulses (at $V_{\text{read}} = 4$ V) with varied pulse amplitudes and pulse widths. b) Schematic plot showing the pulse sequence of a single cycle of potentiation and depression operation. The cycle consists of 20 identical set pulses with 8 V amplitude and 30 ms pulse width followed by 15 reset pulses with a pulse width of 5 ms and progressively increasing amplitudes (starting with -100 mV amplitude with an increase of 100 mV magnitude for every subsequent pulse). c) Potentiation and depression characteristics for 3 cycles. d) Cumulative probability of each state showing a stable and narrow distribution for 100 cycles.

observed for current levels above 100 nA while the lower current levels exhibit high variability in the depression cycles. Despite the degradation observed over cycling, the multi-level operation in both potentiation and depression remains preserved. In Figure 6b the cumulative distribution of the various states over 10³ cycles is shown with the deviation of each state during cycling. To emphasize the maximum number of usable distinct states, overlapping states are removed. Twelve and eleven distinct states are observed during potentiation and depression, respectively. Therefore, a 3-bit per cell memory can be achieved. Although the stack shows degradation in certain states during cycling, its ability to maintain several distinct states through multiple cycles underscores its robustness and potential for application in neuromorphic computing.

2.4. Retention

Typical retention characteristics of the devices are presented in Figure 7. The devices were set to LRS by applying twenty consec-

utive 8 V pulses with a pulse width of 50 ms. The current levels were then measured using a 4 V, 10 ms read pulse. In LRS the current level decays according to a power law ($I \sim t^{-\beta}$) while the HRS remains stable. As seen in Figure 7 the decay follows two distinct slopes: Up to ≈ 100 s the behavior is proportional to $t^{-0.13}$, then it changes to $t^{-0.30}$. The first region may suggest that the decay is associated with the trapping/de-trapping of charge carriers at the interface shortly after switching to LRS.^[9,22,52] The decay of intermediate states is also characterized by a power law ($I \sim t^{-\beta}$), where β decreases gradually for states with higher resistance (shown in Figure S6, Supporting Information). In the second phase ($t > 100$ s) an ionic movement driven mechanism dominates. During switching, oxygen vacancies are expected to move from the GaO_x layer into the TiO_x layer. The increased number of oxygen vacancies in the TiO_x layer leads to the lowering of the effective barrier and to the switching of the device to LRS. Once the device is set to LRS, the oxygen vacancies start to drift back into the GaO_x layer which causes a decay in the current level. Both mechanisms, charging/discharging of traps and drift of oxygen vacancies contribute to the retention loss in LRS but the

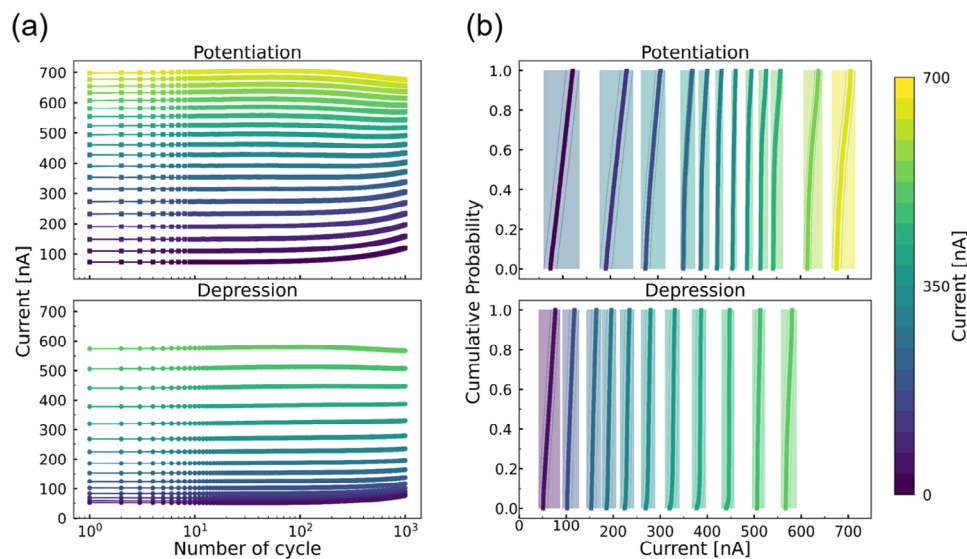


Figure 6. Multiple resistance state endurance: a) Current levels as a function of cycles for potentiation and depression measurements. b) Cumulative distribution of the various resistive states over 1000 potentiation/depression cycles shown together with their deviation in light color. Overlapping states are removed to highlight the maximally usable number of distinct states.

retention loss is minor. Indeed, clearly separated HRS and LRS states are observed even after 5000 s.

3. Conclusion

We demonstrate a non-filamentary memristive Ti/GaO_x/W device where an amorphous sub-stoichiometric GaO_x layer is deposited at a low temperature (250 °C) using PE-ALD. The low-

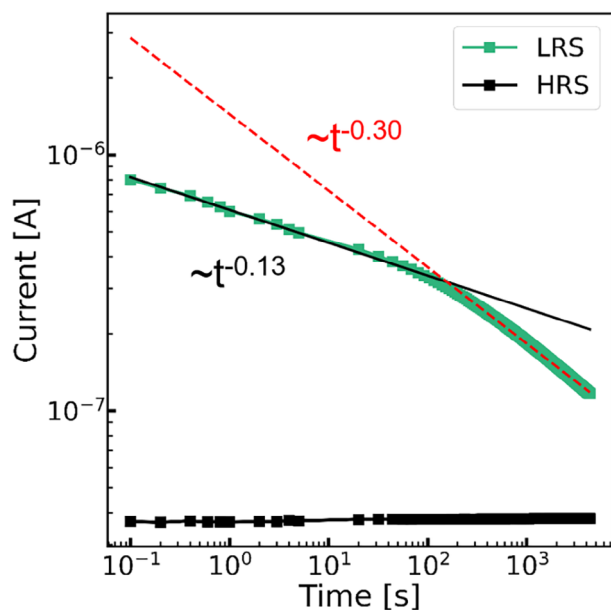


Figure 7. Retention characteristics. Time dependence of the current (at 4 V read bias) in LRS (green data points) and HRS (black data points). The red dashed line and linear black line are the data fits to the power law for the decay of the LRS.

temperature process flow offers high compatibility for integration in the back-end-of-line on a CMOS chip. The device does not require any forming step and shows self-rectifying behavior. The resistance values both in high and low resistance states scale with the electrode area. This indicates that switching takes place over the entire area, pointing to an interfacial/bulk resistive switching mechanism. TEM and EDX studies reveal that the deposition of the GaO_x layer using O₂ plasma on Ti results in the formation of a few nanometer-thick interfacial TiO_x layers. The comparison of devices with different bottom electrodes shows a clear indication for the key contribution of the interfacial oxide in the resistive switching behavior. The mechanism proposed relies on a field driven oxygen vacancy exchange between the GaO_x and TiO_x layers. The devices exhibit multiple resistive states with an endurance of over 1000 cycles and high cycle-to-cycle reproducibility. About twelve stable distinct intermediate states during potentiation and eleven one during depression are demonstrated up to a thousand cycles. This a-GaO_x-based memristive device offers high tunability as PE-ALD process parameters can be adjusted to change the oxygen vacancy content. They can be integrated in 3D structures. Owing to the robust intermediate state stability over cycles (2% dispersion for several states), and their programmability under the sequence of identical pulse amplitude, these devices have a high potential for neuromorphic applications to emulate biological synapses with controllable synaptic weight. However, for such applications, the Set voltage should be significantly reduced for energy efficiency. One approach could be the design of bilayer stacks, combining a thinner GaO_x of a few nanometers with a thin dielectric like HfO₂ or Al₂O₃.

4. Experimental Section

Sample Fabrication: A 60 nm W layer was first sputtered at room temperature on a p++ Si substrate covered with a 300 nm thermal insulating SiO₂ layer. Then, a 40 nm Ti bottom electrode was deposited on top by

thermal evaporation. A 30 nm thick amorphous sub-stoichiometric GaO_x layer was then deposited at 250 °C by plasma-enhanced atomic layer deposition using Ga(CH₃)₃ (Trimethylgallium) as a precursor and O₂ plasma as an oxidizing agent²⁵. The plasma exposure time during GaO_x deposition was of 8 s. A few devices were also fabricated with GaO_x grown using 1s O₂ plasma time to increase the oxygen vacancies content in GaO_x²⁵. TiN and Pt were also investigated as the bottom electrode. Both TiN (30 nm) and Pt (30 nm) were deposited at room temperature by sputtering. The growth of GaO_x on the Ti or TiN bottom electrode resulted in the formation of an interfacial TiO_x or TiO_xN_y interfacial layer respectively. Since GaO_x was etched by the solution used to develop the resist during lithography (AZ 726MIF developer), a special process was required to pattern the top electrode instead of using lift-off. To that end, a blanket W (60 nm) layer was deposited at room temperature by sputtering. Then 20 nm Ti (for adhesion) and 50 nm Au were deposited by thermal evaporation on the blanket W and patterned by lift-off to serve as a hard mask for the tungsten wet etch. Then W was etched at 50 °C in 30% H₂O₂ solution. More than 200 devices were fabricated with active device areas ranging from 30 × 30 to 100 × 100 μm². Finally, a border of the samples was immersed in AZ 726MIF solution to etch the GaO_x layer to give access to the bottom electrode.

Structural Characterization: TEM and EDX analyses. A TEM lamella was prepared from the center of a 100 × 100 μm² device using a Zeiss Crossbeam 340 focused ion beam (FIB). Prior to milling, thin films of Pt were deposited first by e-beam and subsequently by ion beam deposition to protect the device layers from ion beam damage. The lamella was cut parallel to the sample edge. Microscopy experiments were done using a Zeiss LIBRA 200 FE transmission electron microscope (TEM/STEM), operated at 200 kV. The TEM/STEM was equipped with an in-column energy filter which is used to obtain zero-loss filtered images. EDX analyses were done using a Thermo Noran System Six detector and accompanying electronics in STEM mode. The obtained spectra were deconvoluted using the respective routines of the EDX software. The images depicted the number of net counts per pixel.

Optical Characterization: The optical properties of amorphous GaO_x thin films were characterized using spectroscopic ellipsometry. Measurements were conducted on a J.A. Woollam M2000 ellipsometer setup and were performed at three incidence angles (60°, 65°, and 70°) over a wavelength range of 192–1169 nm. To extract the optical constants (refractive index (*n*) and extinction coefficient (*k*)), the experimental data were fitted using a model that combines Tauc–Lorentz and Gaussian oscillators. This approach captured both the bandgap dispersion (via the Tauc–Lorentz oscillator) and sub-bandgap absorption (via the Gaussian oscillator).

Electrical Characterization: The electrical characterization was performed on an MPI TS2000-SE probe station with a Keysight B1500A semiconductor parameter analyzer. All signals were applied to the W top electrode and the Ti (or TiN or Pt) bottom electrode was grounded. Voltage–current measurements were performed on devices with different contact areas: 30 × 30, 50 × 50, 70 × 70, and 100 × 100 μm². For the Set operation the voltage was swept from 0 to 8 V with a sweep rate of 4 mV s⁻¹, for Reset from 0 to -1.5 V with a sweep rate of 1.7 mV s⁻¹. The pulsed measurements were conducted utilizing a Keysight B1530A waveform generator/fast measurement unit (WGFMU), which is a plug-in module for the Keysight B1500A semiconductor parameter analyzer.

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

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Conflict of Interest

The authors declare no conflict of interest.

Data Availability Statement

The data that support the findings of this study are available from the corresponding author upon reasonable request.

Keywords

gallium oxide, interfacial switching, memristive device, non-filamentary, resistive switching

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