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Quantification of Interfacial Charges in Multilayered Nanocapacitors by Operando Electron Holography

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Interfaces in heterostructures play a major role in the functionality of electronic devices. Phenomena such as charge trapping/detrapping at interfaces under electric field affect the dynamics of metal/oxide/metal capacitors and metal/oxide/semiconductor transistors used for memory and logic applications. Charge traps are also key for the stabilization of a ferroelectric polarization and its ability to switch in ferroelectric devices such as ferroelectric tunnel junctions (FTJs). However, electric-field induced charging phenomena remain unclear even in conventional dielectric heterostructures due to a lack of direct measurement methods. Here, it is shown how operando off-axis electron holography can be used to quantify the charges trapped at the dielectric/dielectric interfaces as well as metal/dielectric interfaces in HfO_2- and Al_2O_3-based nanocapacitors. By mapping the electrostatic potential at sub-nanometer spatial resolution while applying a bias, it is demonstrated that these interfaces present a high density of trapped charges, which strongly influence the electric field distribution within the device. The unprecedented sensitivity of the electron holography experiments coupled with numerical simulations highlights for the first time the linear relationship between the trapped charges at each interface and the applied bias, and the effect of the trapped charges on the local electrical behavior.

1. Introduction

The development and improvement of micro and nanoelectronic devices generate considerable attention in applied and fundamental research. In particular, the integration of new materials enables devices to be optimized in speed and power consumption. Among these, high-κ materials are being actively investigated for their robust properties, including not only their high dielectric permittivity, but also their high thermal stability and good compatibility with complementary metal-oxide-semiconductor (CMOS) technologies. E.g., HfO_2 has been integrated into field-effect transistors (FETs) as a gate oxide in place of SiO_2 to allow the further decrease of the device dimensions with an acceptable level of leakage currents.[1,2] The use of HfO_2 has thus successfully limited the static power consumption of transistors due to quantum mechanical tunneling with the shrinking of transistor dimensions.[3] Al_2O_3 is another prominent dielectric in nanoelectronics. It is used as a dielectric layer in memory devices (such as dynamic random access memories), as a charge trapping layer in nonvolatile memories (such as flash memories), as a tunneling barrier in magnetic and ferroelectric tunnel junctions (FTJs), as a gate insulator in thin film transistors and as a passivation or encapsulating layer in various devices (solar cells, optoelectronic devices).

HfO_2 and Al_2O_3 are also key oxides for non-volatile resistive random-access memory (RRAM) devices. Such devices allow the emulation of biological synapses to conceive energy-efficient neuromorphic computing systems[4] as a solution to the bottleneck of traditional computing systems based on classical von Neumann architectures.[5,6] During operation of a RRAM device, the low and high resistance states of the two-terminal metal/insulator/metal (MIM) memory cell can be switched by the application of electrical stimuli. The ionic motion under the electric field, as well as the creation and motion of defects such as oxygen vacancies, can lead to the formation and breakage of conductive filaments in the oxides, local redox reactions, or modification of the metal-insulator barrier.[7–14] While pure HfO_2[15,16] or Al_2O_3[17–19] layers exhibit non-volatile resistive switching characteristics, RRAM devices containing bilayer[12,20–22] or multilayer[23–26] alternating HfO_2 and Al_2O_3 are

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very promising for memristive memory applications. E.g., Rao et al.[22] have achieved 2 048 conductance levels in a bilayer HfO_2/Al_2O_3-based memristor on a fully integrated chip. Charge trapping plays an important role in the resulting properties. It was reported that, during switching, the trapping and de-trapping of carriers via interfacial or bulk trap sites may be responsible for the variable resistance states,[23,27] the programing/erase parameters,[28,29] and the endurance reliability issue.[28,30] However, their exact locations are a matter of debate, in which some reported a trapping in the oxide layers[31,32] while some others indicated a charge trapping at the interfaces (between the oxide/nitride layers[33,34] or between Al_2O_3 and the metal gate).[35,36] It was also claimed that the trapped charges can be confined both in the bulk HfO_2 layer and at the HfO_2/Al_2O_3 interface.[27] As a function of the applied bias, some traps are expected to be stable over time and others are occupied dynamically, but it remains a difficult task to distinguish these charges.

Moreover, it is important to mention that HfO_2-based compounds (doped HfO_2,[37–39] $Hf_{0.5}Zr_{0.5}O_2$ or HZO)[40,41] are extensively investigated for several years for their ferroelectric properties and their applications as ferroelectric capacitors, FETs and FTJs.[42] In bilayer HZO-based FTJs, a thin Al_2O_3 layer is used as a tunnel barrier. Modeling of the polarization and current characteristics as a function of applied bias has evidenced the central role of charge trapping in these devices.[43–47] Charge trapping is central to the development of a sizable polarization and in the related depolarization field[48–51] and therefore requires a deep understanding for the exploitation of ferroelectric (or negative capacitance) devices. It is therefore unfortunate that, despite their key role, charges trapped at the interface between these dielectric materials have never been directly measured.

Quantitative measurement of interfacial charges at the nanoscale has long been a challenging task due to a lack of spatial resolution and/or a lack of sensitivity for most techniques, including the Fermi probe technique, thermal activation, photoemission, in situ X-ray photoelectron spectroscopy and electron spin-based methods.[52] However, transmission electron microscopy (TEM) allows samples to be investigated in cross-sectional geometry with a very high spatial resolution, which is required to study phenomena precisely through an entire device or a sequence of layers. Few TEM methods are capable of measuring electric fields. While most recent attention has been focused on 4D scanning transmission electron microscopy (4D-STEM),[53] electron holography is a powerful interferometric TEM technique that is less sensitive to diffraction contrast and does not need large data sets,[54] making it particularly suitable for in situ studies. However, very few examples of in situ electron holography have been reported for the study of charges at the interfaces between oxides, such as high-κ oxides for charge trapping memories[34] or perovskite oxides which present a modulation of 2D electron gas.[55] In these studies, the charge quantification is limited by the sensitivity to the phase shift and the role of leakage field. In a previous work, we used a recently developed methodology based on off-axis electron holography to study the potential distribution across a working MOS nanocapacitor containing a single SiO_2 layer as a function of a DC voltage.[56] We revealed an unexpected interfacial charge density within the dielectric at the immediate vicinity with the electrodes proportional to the applied bias voltage. This trapped charge layer was shown to extend over a distance larger than the structural or chemical width of each interface.

Here, we address this key aspect for nanoelectronic, optoelectronic and photovoltaic device optimization, namely the quantification of charge traps at the interfaces between two dielectrics under an applied bias. For this purpose, we have designed two nanocapacitors with three dielectric layers, $TiN/HfO_2/Al_2O_3/HfO_2/TiN$ and $TiN/Al_2O_3/HfO_2/Al_2O_3/TiN$ and improved the sensitivity to the phase shift of our setup by using a direct electron detector combined with long exposure times and a smart acquisition process.[57] In this way, we have studied with sub-nanometric spatial resolution the distribution of the electric field and charges at the interfaces between HfO_2 and Al_2O_3, as well as at the metal/dielectric interfaces, as a function of the voltage applied in situ. We show that the presence of trapped charges at the dielectric/dielectric interfaces tends to uniformize the electric field distribution throughout the whole dielectric stack while the charged metal/dielectric interfaces screen a part of the applied electric field, leading to a lower effective field inside the stack. The quantification of related charge densities evidences a linear relationship with the applied bias and the variation in permittivity between the dielectrics.

2. Results

2.1. Architecture of Nanocapacitors

Figure 1a,e shows the designed twin trilayer dielectric nanocapacitors under investigation: $TiN/HfO_2/Al_2O_3/HfO_2/TiN$ (stack A) and $TiN/Al_2O_3/HfO_2/Al_2O_3/TiN$ (stack B). The details of the thin film growth, characterization, and nanocapacitor fabrication are given in the Experimental Section. The TiN layers correspond to the top and bottom electrodes. The thicknesses of the HfO_2 and Al_2O_3 layers measured from TEM micrographs are 23 nm and 20 nm, respectively. In our approach, the nanocapacitor B has a stack symmetrical to that of nanocapacitor A, making it possible to distinguish between the electrical contributions of the metal/dielectric interfaces, specific to each system, from those of the dielectric/dielectric interfaces present in each system. Both systems have been elaborated on a highly *p*-doped Si (10^{18} atoms·cm^{-3}) substrate used for the back contact.

TEM observations were carried out to verify the structural and chemical quality of the different layers, focusing on the interfaces. The images in Figure 1b,f show the active regions of A and B nanocapacitors, respectively, with uniform and well-defined layers. The spatially-resolved chemical compositions of each interface determined by energy electron loss spectroscopy (STEM-EELS) analysis are presented (see Figures S3–S5, Supporting Information). All interfaces appear quite sharp and flat, whether we consider structural or spectroscopic investigations. A chemical intermixing region of Ti oxinitride (TiO_xN_y) with some amount of Hf or Al atoms is observed at the TiN/dielectric interfaces for both nanocapacitors while the dielectric/dielectric interfaces present a narrow transition region. All interfaces have a homogenous width ≈3.0 nm, except for the top TiN/Al_2O_3 interface with a thickness of ≈5.0 nm in nanocapacitor B. It should be noted here that the relatively low interface thickness measured may be due to slight chemical mixing and/or a projection effect linked to the thickness of the lamellae.

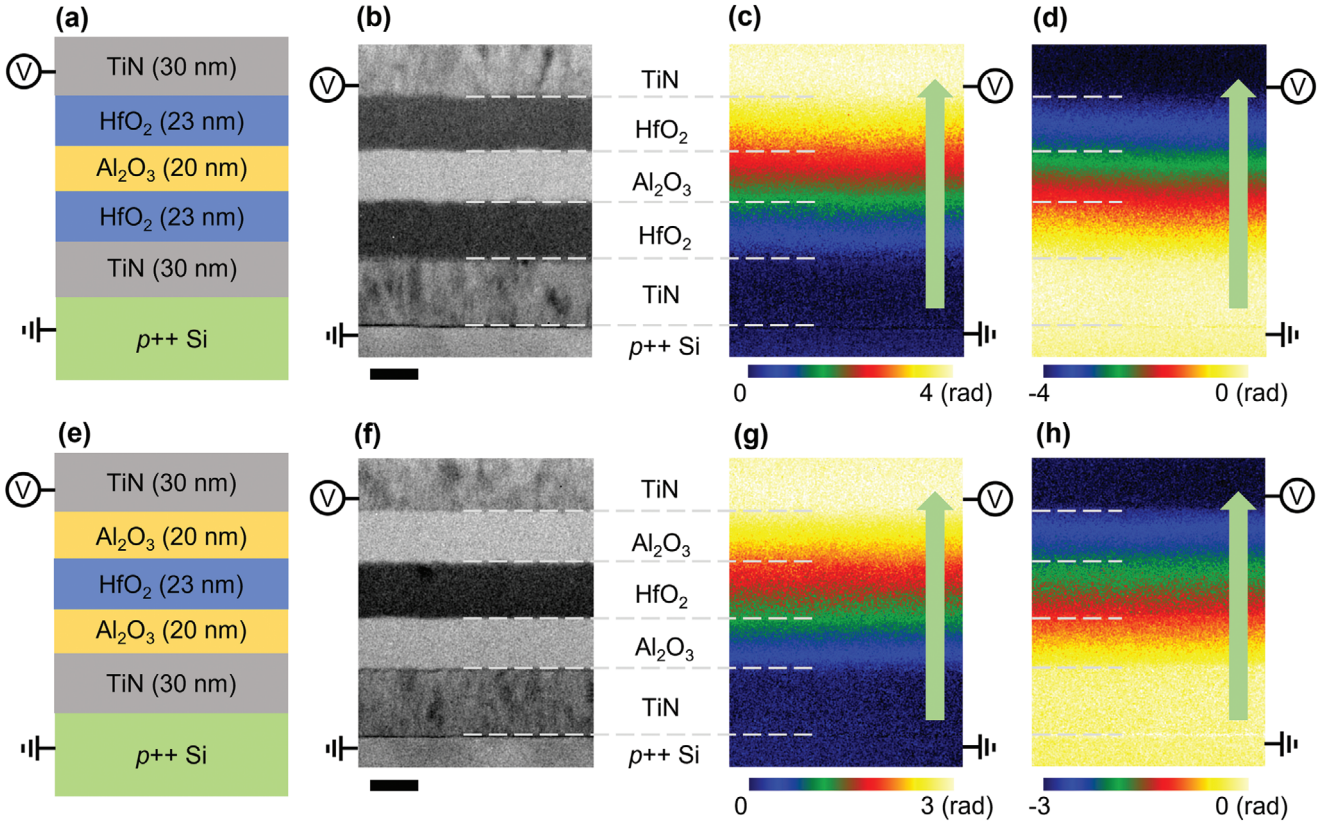

Figure 1. Sketches, amplitude, and phase images of the twin trilayer nanocapacitor devices containing high-κ Al_2O_3 and HfO_2 dielectrics. a,e) Sketches of stack A: $HfO_2/Al_2O_3/HfO_2$ and stack B: $Al_2O_3/HfO_2/Al_2O_3$. b,f) Amplitude images respectively showing the different layers of the nanocapacitors A and B. c,g) Phase maps of projected electric potential on the same area obtained by electron holography for the nanocapacitors A and B with an applied bias of +6 V. d,h) Phase maps for the nanocapacitors A and B with an applied bias of -6 V. Scale bars are 20 nm in (b) and (f).

2.2. Operando Electron Holography Experiments

Specific specimen-devices for operando electron holography experiments were prepared in cross-sectional geometry using advanced focused ion beam (FIB) processing. Each nanodevice is electron transparent and electrically contacted to a chip that is inserted into a dedicated biasing holder (details can be found in the Supporting Information). This approach has major advantages over a dedicated probe-based approach[58] where the stray field around the nanoprobe is significant and the contact resistance between the nanoprobe and the electron transparent lamella is difficult to control. The strong stray field from a contact probe would also affect the measurement by perturbing the reference area of the hologram as well as the potential applied to the active area.[59,60] A probe contact can also cause mechanical instability. In comparison, the specimen-device with the specific sample geometry used here avoids the problems associated with a nanoprobe contact and works in a very similar way to a real device where the nm-sized active area is submitted to the macroscopically applied bias. Under the applied DC bias, the chip and the Hummingbird holder allow the electric field to be applied directly on the top and bottom TiN electrodes. Although TEM setup modifies the geometry or the aspect ratio (between electrode and dielectric layers) of the structure of the specimen device, the chemical composition and thickness values of each dielectric layer remain the same. This makes our measurement quite similar to the real case we would like to evidence the interface charge trapping behavior in its quasi-equilibrium state, which reflects the "operando" circumstance. In the following, the bottom electrode (TiN layer deposited on the Si substrate) is grounded and the potential is applied to the top electrode.

The principle of electron holography is to interfere a highly coherent electron beam that has interacted with the specimen, the object wave, with a reference wave that has not undergone any interaction.[61,62] The resulting interference pattern (i.e., the hologram) contains all of the information about the phase shift ϕ of the electron wave experienced with the local electric and magnetic potentials. The analysis of the resulting phase shift allows quantitative mapping of the potentials with a sub-nanometric spatial resolution.[63–67] In our case where no magnetic contribution is expected, the phase shift is only related to the electrostatic potential $V(x, y, z)$ encountered by the fast electrons along their trajectory:[68]

$$\phi(x, y) = C_E \int V(x, y, z)\, dz \tag{1}$$

where x,y are the directions in the image plane, z the direction parallel to the electron beam and C_E a constant depending on universal constants and the accelerating voltage of the microscope ($C_E = 6.53 \times 10^6$ V^{-1} m^{-1} at 300 kV).[68]

However, V is the sum of a static contribution, the mean internal potential (MIP) of the material, and the electrical potential created by the bias, the quantity to be measured. These contributions to the phase shift, which we will refer to as ϕ_{MIP} and ϕ_{Bias}, respectively, must therefore be separated. For this purpose, our methodology combines the advanced FIB preparation process and operando electron holography experiments where the device is biased or grounded during the observations.[56,69] Upon biasing, ϕ_{Bias} is created by the stray fields around the specimen device as well as the electrical potential within the specimen device while ϕ_{MIP} is measured by recording a hologram with the electrodes being grounded.

We thus applied different DC biases, ranging from −12 to +12 V, to the nanocapacitor A while recording holograms. Several holograms were periodically acquired with both electrodes grounded (0 V) to measure ϕ_{MIP} and to ensure that no change occurred during the experiment. The phase images extracted from these holograms with grounded electrodes were used as references and subtracted from other phase images to remove the MIP contribution to the phase shift and all unwanted static contributions such as damage layers, diffraction contrast, and electron beam induced charging.[70,71] The remaining signal can then be attributed only to the phase contribution ϕ_{Bias} created by the applied bias. However, as ϕ_{Bias} is also sensitive to the stray fields around the sample, modeling is essential to obtain the electrical potential within the sample and reliable quantitative results. The same procedure was used for the nanocapacitor B but with a bias between −6 and +6 V, the sample being damaged at a higher value.

Examples of resulting phase images corresponding only to ϕ_{Bias} with an applied bias of +6 V for A and B are shown in Figure 1c,g, respectively. And the phase images at a bias of −6 V are displayed in Figure 1d,h, respectively for A and B. A specific region within the bottom TiN electrode was used as the reference area where the phase shift was set to 0.

The phase images for all applied biases are reported in Figures S6 and S7 (Supporting Information), respectively, for nanocapacitors A and B. The phase profiles across the stacks A and B (direction given by the green arrows in Figure 1c,d,g,h) for all applied biases are reported in **Figure 2**a,b, respectively. They were averaged over a length of 120 nm parallel to the interfaces to improve the signal-to-noise ratio and to reach a phase noise lower than 10 mrad in the TiN bottom electrode for a spatial resolution of 0.67 nm.

2.3. Analysis of the Phase Profiles

The phase profiles in Figure 2a,b show the variation of the projected electrical potential for different applied biases. As expected, the total phase shift between the two TiN electrodes increases linearly with increasing bias voltage for both nanocapacitors and the profiles appear symmetric when the sign of the bias is switched, for example from +6 to −6 V.

A gradient in the electrostatic potential results in an electric field. As expected, all the TiN contact layers appear to be at a uniform potential for both nanocapacitors A and B. The phase profiles show a slight curvature in the TiN layers due to the stray field above and below the specimen-device.[56,72] On the other hand, there is a clear gradient in the phase within the dielectric layers indicating the presence of an electric field. However, dielectrics of different permittivity should have different electric fields: it is thus very surprising that all the phase profiles in Figure 2a,b for both nanocapacitors A and B display similar gradients within the Al_2O_3 and HfO_2 layers suggesting an equiv. electric field distribution. This important result implies the presence of additional charges trapped at the interfaces between the dielectrics.

To better quantify the charge and potential distributions, we carried out extensive finite element method (FEM) modeling, considering not only the specimen geometry (lamella thickness, width of each layer) deduced from TEM observations and the relative permittivity of each dielectric, but also the existence of charged layers within the dielectrics or at the interfaces. For each applied bias, the potential inside the specimen-device and the stray field were determined by FEM and used to calculate the simulated phase profiles by applying Equation 1. The relative permittivities $\varepsilon_{HfO_2} = 18$ and $\varepsilon_{Al_2O_3} = 7.4$ for amorphous HfO_2 and Al_2O_3, respectively, used in the model were determined from C-V measurements on macroscale capacitor devices ($95 \times 95\ \mu m^2$) as shown in Figure S8 (Supporting Information). The other parameters introduced into the FEM simulations (lamella thickness, applied bias, width, position, and volume charge density of charged layers) were adjusted until the best agreement with the experimental profiles was reached. For instance, the lamella thicknesses, measured at 52 ± 5 nm and 43 ± 4 nm for the nanocapacitors A and B, respectively, using the MIP contribution of Si substrate, were set to 55 nm and 40 nm, respectively, in the best fitting.

The experimental and simulated phase profiles corresponding to an applied bias of +6 V are shown in Figure 2b,e for the nanocapacitors A and B, respectively. We can see that the simulated profiles using an electrostatic model without introducing charge layers (green curve) cannot account for the experimental results for any of the samples (black curves). In this case, the simulated electric field is significantly higher in the Al_2O_3 layer than the one in the HfO_2 layer, which was not observed experimentally. However, by adding positive and negative charged layers at the interfaces, a near-perfect fit can be achieved (red curves).

More precisely, the best agreement is obtained when four charged interfacial layers are introduced as illustrated schematically in Figure 2. In the FEM simulations, we considered uniformly charged interfacial layers of 3 nm, except for the Al_2O_3/TiN interface of B with a width of 5 nm. These widths are comparable to those measured by STEM-EELS when studying the chemical composition at the interfaces (see Figures S3–S5, Supporting Information). The charge density at each interface was carefully adjusted until the simulated profile reproduces nicely the experimental profile. Owing to their small width, we will consider these interfaces in the following as being surface charged. The corresponding surface charge densities are denoted σ_{A1}, σ_{A2}, σ_{A3}, σ_{A4} for A and σ_{B1}, σ_{B2}, σ_{B3}, σ_{B4} for B. Here, σ_{A1}, σ_{A4}, σ_{B1}, and σ_{B4} are for metal/dielectric interfaces while σ_{A2}, σ_{A3}, σ_{B2} and σ_{B3} correspond to dielectric/dielectric interfaces as represented in Figure 2.

Note that the local applied bias in the best-fitting models shown in Figure 2b,e was adjusted to +5.71 V and +5.61 V for

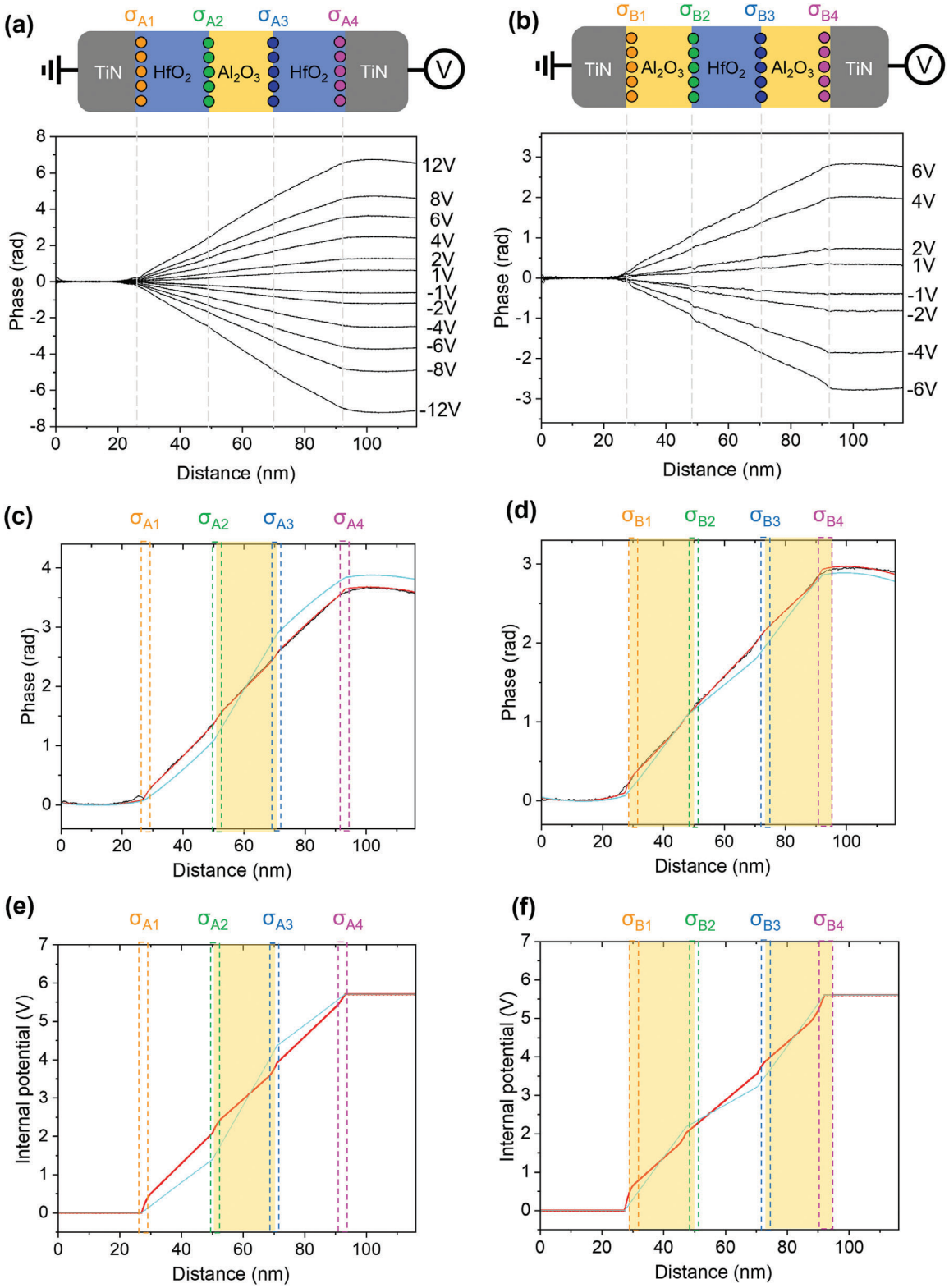

Figure 2. Experimental phase profiles and FEM simulation profiles as a function of applied bias for the nanocapacitors A and B. a,b) Experimental phase profiles for A and B, respectively. c,d) Phase profiles at a bias of +6 V for A and B, respectively: experimental in black, FEM simulation with charged interfacial layers in red, FEM simulation without charged layers in light blue. e,f) Internal electric field profiles for A and B, respectively, extracted from FEM simulations with (in red) and without (in light blue) the charged layers at a bias of +6 V. The locations of the charged interfaces, with charge densities σ_{A1}, σ_{A2}, σ_{A3}, σ_{A4} for A and σ_{B1}, σ_{B2}, σ_{B3}, σ_{B4} for B, respectively, are marked by the dotted rectangles on the profiles.

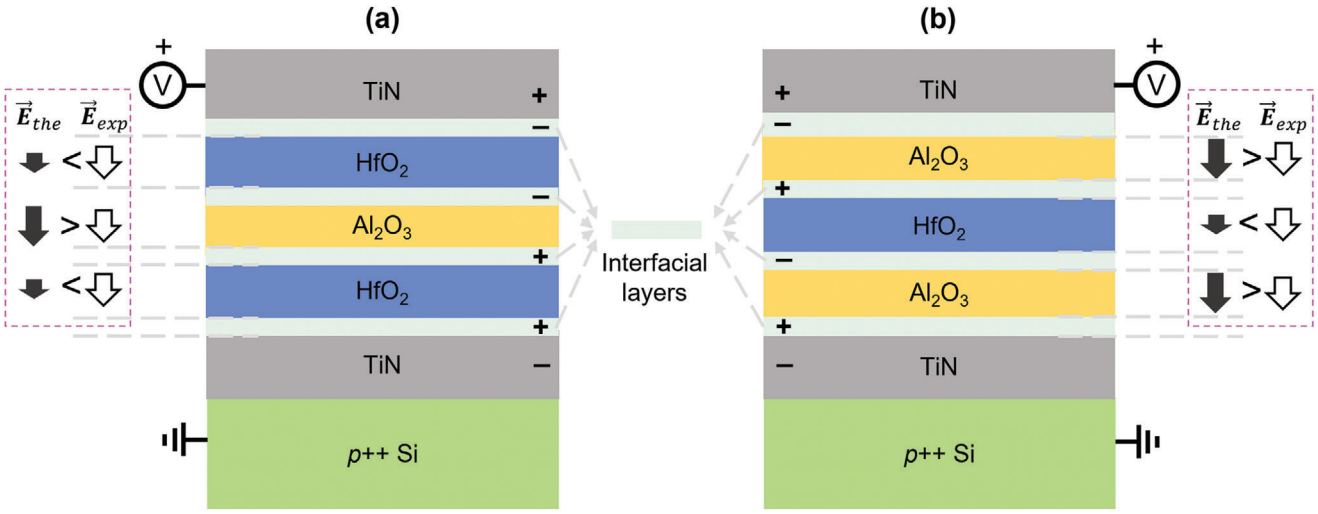

Figure 3. Electric field distributions of the trilayer nanocapacitor devices upon positive bias: a) A; b) B. For both nanocapacitors, the electric fields, $\vec{E}_{exp}$ (in white arrows), strongly deviate from the theoretical ones, $\vec{E}_{the}$ (in black arrows), due to the presence of trapped free charges ("+" or "-") at the four interfacial layers. Bound dielectric charge is not shown.

A and B, respectively. These values are slightly smaller than the macroscopically applied voltage of +6 V indicated by the external supply during the experiment. If the dominant source of uncertainty in the FEM simulations is the lamella thickness, the slight discrepancy between the local and macroscopic bias can also be caused by leakage currents and series resistance in the connections.

It is also interesting to point out that the location of the charged interfacial layers determined in the FEM simulations can be slightly shifted with respect to the interfaces seen structurally or chemically according to the TEM experiments: the charge areas at the metal/dielectric interfaces are located in the dielectric in the immediate vicinity of the metal, whereas the charged areas at the dielectric/dielectric interfaces are in the chemical transitioning region between Al_2O_3 and HfO_2 whatever the stacking order is.

FEM modeling enables the internal and external (stray field) contributions to the phase shift to be separated (see Figure S9, Supporting Information). The resulting profiles for the potential inside the specimen-devices are shown in Figure 2e,f for the nanocapacitors A and B, respectively. They all confirm that the internal electric field is indeed zero in the TiN electrodes with a uniform potential and that the curvature of the phase in the regions corresponding to the electrodes is caused by the stray fields around the thinned sample for both specimen-devices. The effect of the trapped interfacial charges on the internal electric field is highlighted on the profiles. Without the charged interfaces (blue curves), the electric field, i.e., the slope of the potential profile, should be greater in Al_2O_3 than in HfO_2 by a factor equal to the ratio of the relative permittivities $\frac{\varepsilon_{HfO_2}}{\varepsilon_{Al_2O_3}}$ (2.43 in our case). In contrast, the profiles with charged interfaces calculated from the best agreement with the experimental results (red curves) present similar electric fields in all the dielectric layers, and for both nanocapacitors. The interfacial charges create a confined curved potential step at each interface and homogenize the electric field in both Al_2O_3 and HfO_2 layers. The same conclusion can be drawn by considering the profiles simulated with a bias of -6 V (see Figures S10 and S11, Supporting Information).

From the simulated potential profiles in Figure 2e,f obtained with an applied bias of +6 V, we calculated an average internal electric field of 7.6×10^5 V cm^{-1} for A and 6.9×10^5 V cm^{-1} for B within the dielectrics, excluding the interfacial layers where the fields can be much higher. These values are lower than the field applied by the electrodes considering the total thickness (66 nm and 63 nm for A and B, respectively) and the local bias determined by FEM modeling (5.71 V and 5.61 V, respectively). The applied electric field should then be 8.65×10^5 V cm^{-1} for A and 8.9×10^5 V cm^{-1} for B. This reduction is explained by the charges at the TiN/dielectric interfaces, which partially screen the field generated by the bias. We observed the same effect of these interfacial charges near the electrodes in a $Si/SiO_2/Ti$ capacitor studied using the same methodology.[56]

Figure 3 shows sketches for both nanocapacitors with the location of all trapped charges and their signs for a positive bias, as well as the resulting electric field distributions, which are compared with the theoretical ones without charged interfaces. The bound dielectric charge is not shown.

As we have seen, in the absence of charged interfaces, the internal electric field should be much higher in Al_2O_3 than in HfO_2, and for both nanocapacitors A and B. The difference in electric field is caused by the difference in dielectric permittivity, leading to a net bound dielectric charge at the internal interfaces. Experimentally, on the other hand, the electric field within the HfO_2 and Al_2O_3 layers is very similar. The uniformization of the electric field can only result from a trapping of free charges at the internal interfaces: the trapped charge compensates the net bound charge from the dielectric polarization and is necessarily of opposite sign. As a result, the net charge, including free and bound charges, is almost zero on the internal interface. This explains why the same type of interface can have trapped charges of different signs. It is the stacking order and the sign of the

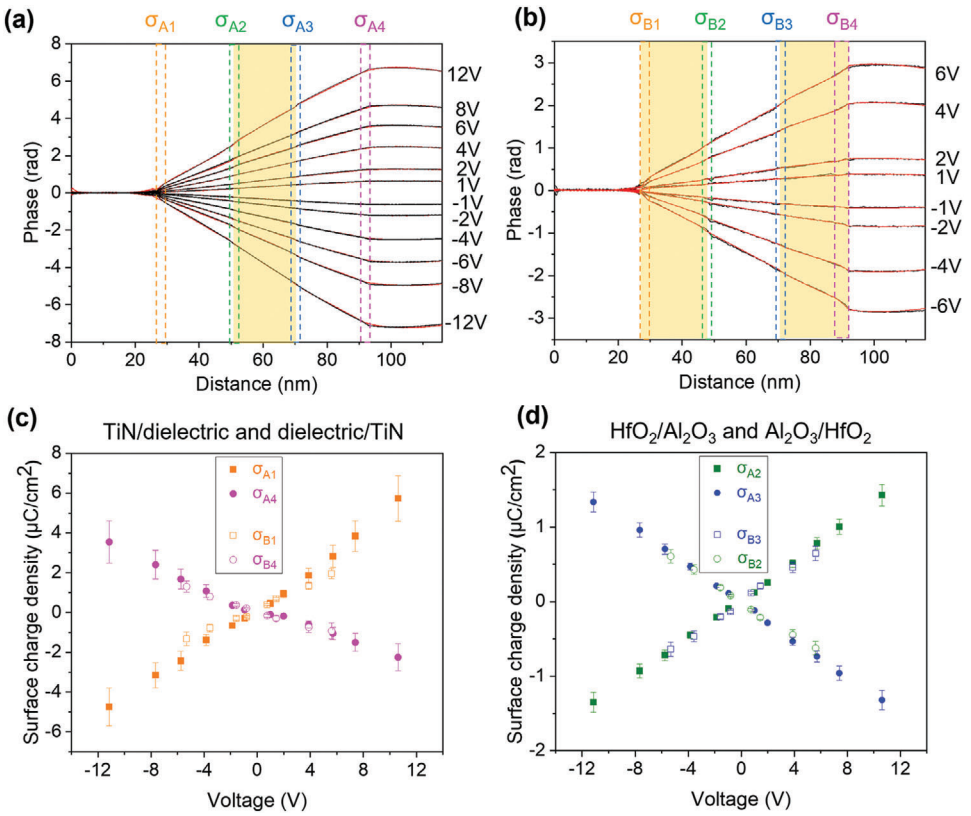

Figure 4. a,b) Experimental phase profiles and FEM simulation profiles for all applied biases for the nanocapacitors A and B, respectively. c,d) Interfacial charge densities as a function of the applied bias for the nanocapacitors A and B: c) TiN/dielectric and dielectric/TiN interfaces; d) HfO_2/Al_2O_3 and Al_2O_3/HfO_2 interfaces.

applied voltage that determines the sign. On the other hand, the sign of the trapped charges at the interface between the electrode and the dielectric depends solely on the applied voltage and is opposite to that of the free charges of the neighboring electrode.

At this point, it is necessary to treat the charged interfacial layers separately according to their type: the free charges at the dielectric/dielectric interfaces (σ_{A2}, σ_{A3}, σ_{B2}, and σ_{B3}) tend to equalize the electric field within the dielectrics while the charges at the metal/dielectric interfaces (σ_{A1}, σ_{A4}, σ_{B1}, and σ_{B4}) reduce the average field within all the dielectric layers.

2.4. Interfacial Charge Quantification

As seen in **Figure** 4a,b, through carefully adjusting the charge density at each interface and for each bias on the FEM simulations, we were able to reproduce accurately the complete set of experimental profiles for both nanocapacitors A and B. The potential loss ΔV, defined as the difference between the macroscopic value and the local bias determined by the simulations, was observed for nearly all the simulated profiles (see Figures S12 and S13, Supporting Information) and its variation with the applied bias seems to confirm an origin from leakage currents.

The values of the equiv. surface charge densities introduced in the FEM modeling to fit the experimental data for all applied biases are presented in Figure 4c,d for both nanocapacitors A and B. Figure 4c corresponds to the surface densities of the trapped charges at the metal/dielectric interfaces while Figure 4d shows those at the dielectric/dielectric interfaces. The error bars reflect the uncertainties related to the thickness of the lamella and the fluctuation of the experimental phase shift profiles. The same bias convention was used (bottom electrode grounded, applied potential on the top electrode) and the values of the bias on the x-axis were adjusted from those used in the FEM modeling to take into account the potential loss ΔV.

The first thing that stands out is that all interfacial charge densities, negative or positive, vary linearly with the bias, regardless of the trilayer stack. They are generated during the biasing process and we experimentally verified that they do not depend on the bias history by returning to previous bias values from time to time within a cycle. Furthermore, the hologram phase was stable over the acquisition time at each particular bias. All these observations suggest that all the interfacial charges within the sample are in a state of equilibrium. However, the charged interfacial layers have a different effect on the internal electric field according to their type, and they also differ in terms of values and variation with the applied bias. **Tables** 1 and 2 summarize the slope of each surface density as a function of bias extracted from the graphs in Figure 4. The slope value represents the charge trapping ability of a certain interface upon biasing. All values are expressed in the unit of μC cm^{-2} V^{-1}.

Table 1. Slope values of surface charge densities for the nanocapacitor A.

TiN/HfO_2 (σ_{A1}/V) $\mu C\ cm^{-2}\ V^{-1}$		HfO_2/Al_2O_3 (σ_{A2}/V) $\mu C\ cm^{-2}\ V^{-1}$	Al_2O_3/HfO_2 (σ_{A3}/V) $\mu C\ cm^{-2}\ V^{-1}$	HfO_2/TiN (σ_{A4}/V) $\mu C\ cm^{-2}\ V^{-1}$	
V<0	V>0			V<0	V>0
0.41 ± 0.06	0.50 ± 0.08	0.13 ± 0.01	−0.12 ± 0.01	−0.30 ± 0.08	−0.20 ± 0.05

3. Discussion

For both specimen-devices, the metal/dielectric interfacial layers have larger trapped charge densities (σ_{A1}, σ_{A4}, σ_{B1} and σ_{B4}) compared to the dielectric/dielectric ones. In these metal/dielectric interfaces, the sign of the trapped charges located in the dielectric layers in the immediate vicinity depends on the applied bias and is opposite to that of the free charges of the neighbouring electrode. In addition, the charge densities present different bias dependences (slopes) according to the sign of the applied bias. More precisely, it is easier to trap positive than negative charges, whatever the dielectric near the TiN electrodes and the stacking sequence of the interface (TiN/dielectric or dielectric/TiN). Chemical defects are a possible origin of this affinity for a given type of trapped charges. The analysis of values given in Tables 1 and 2 also shows that the interfaces near the bottom TiN electrode always present higher densities (σ_{A1} and σ_{B1}) than those near the top electrode (σ_{A4} and σ_{B4}) in a same capacitor, whatever the sign of the trapped charges. This difference is explained by the asymmetry in the elaboration processes: the dielectric is deposited on the bottom TiN electrode, after an air break, and using H_2O oxidant during the ALD process, while for the top electrode, the metal is deposited on the dielectric by sputtering. The two interfaces are of course not equiv. However, it is interesting to note, as mentioned previously, that these two interfaces are very similar from the point of view of structural and chemical properties, and that the charged interfacial layers are located into the dielectric part, presumably the TiO_xN_y layer.

If we now compare the metal/dielectric interfaces between the two systems, the nanocapacitor A (TiN/HfO_2 and HfO_2/TiN interfaces) has higher values of trapped charge densities compared to the nanocapacitor B (TiN/Al_2O_3 and Al_2O_3/TiN interfaces). The ratios between the densities for the same bottom or top interface (σ_{A1}/σ_{B1} or σ_{A4}/σ_{B4}) at the same bias value vary between 1.25 and 1.5, which is very close to the ratio between the capacitances of the capacitors (≈1.3). However, the effect on electric field screening is less significant for A, since the permittivity of HfO_2 in the vicinity of TiN in A is 2.43 times greater than that of Al_2O_3 in B.

The charge densities at the dielectric/dielectric interfaces – lower than those at the metal/dielectric interfaces – have an interesting behaviour with the applied bias. The Figure 4d shows that the σ_{A2} and σ_{A3} curves of A overlap with the σ_{B3} and σ_{B2} curves respectively of B, which is reflected in the identical slopes given in Tables 1 and 2. Unlike the previous case, these values do not change with the sign of the applied bias. These observations indicate that a given interface, say HfO_2/Al_2O_3, behaves in the same way from the point of view of charge trapping, no matter which layer is below HfO_2 (TiN or Al_2O_3). This is expected as the compounds, the processing conditions and nature of defects of these interfaces are the same. However, note that HfO_2/Al_2O_3 and Al_2O_3/HfO_2 interfaces are not strictly equiv.: if they have a similar charge density in absolute values (and similar bias dependence), the sign of the charges depends on the stacking sequence of the interface (HfO_2/Al_2O_3 or Al_2O_3/HfO_2) for a same bias. For a positive voltage where the electric field is oriented from the top electrode to the bottom one, the HfO_2/Al_2O_3 interfaces (σ_{A2} and σ_{B3}) have a positive charge density, contrary to the Al_2O_3/HfO_2 interfaces (σ_{A3} and σ_{B2}). The signs are reversed with respect to the applied bias and hence to the electric field.

The homogenization of the electric field throughout the nanocapacitors also allows a direct analytical approach for calculating the interfacial charges directly and comparing these values with those measured by FEM by adjusting the experimental phase profiles. Considering the electric displacement field D within the capacitors, only normal components at the interfaces exist and the boundary condition is then written as:

$$D_{HfO_2} - D_{Al_2O_3} = \sigma \tag{2}$$

where σ is the free charge density at the interface. The sign of σ depends on the sign of the applied voltage, but also on the stacking sequence of the interface.

In our systems, the electric field is almost the same in every dielectric layer, hence $D_{HfO_2} = \epsilon_0\ \epsilon_{HfO_2} E$ and $D_{Al_2O_3} = \epsilon_0 \epsilon_{Al_2O_3}\ E$ where ϵ_0 is the vacuum permittivity and E the mean value of the electric field. For a positive applied bias, the boundary conditions between the dielectrics then become:

$$\varepsilon_0 E\left(\varepsilon_{HfO_2} - \varepsilon_{Al_2O_3}\right) = \sigma_{A2} \text{ for A} \tag{3}$$

$$\varepsilon_0 E\left(\varepsilon_{HfO_2} - \varepsilon_{Al_2O_3}\right) = \sigma_{B3} \text{ for B} \tag{4}$$

Table 2. Slope values of surface charge densities for the nanocapacitor B.

TiN/Al_2O_3 (σ_{A1}/V) $\mu C\ cm^{-2}\ V^{-1}$		Al_2O_3/HfO_2 (σ_{A3}/V) $\mu C\ cm^{-2}\ V^{-1}$	HfO_2/Al_2O_3 (σ_{A2}/V) $\mu C\ cm^{-2}\ V^{-1}$	Al_2O_3/TiN (σ_{A4}/V) $\mu C\ cm^{-2}\ V^{-1}$	
V<0	V>0			V<0	V>0
0.27 ± 0.05	0.36 ± 0.06	−0.11 ± 0.01	0.12 ± 0.01	−0.24 ± 0.05	−0.13 ± 0.01

and

$$\varepsilon_0 E\left(\varepsilon_{Al_2O_3} - \varepsilon_{HfO_2}\right) = \sigma_{A3} \text{ for A} \quad (5)$$

$$\varepsilon_0 E\left(\varepsilon_{Al_2O_3} - \varepsilon_{HfO_2}\right) = \sigma_{B2} \text{ for B} \quad (6)$$

These relations explain why a sign inversion of the trapped charge density is expected between the HfO_2/Al_2O_3 and Al_2O_3/HfO_2 interfaces, and why the absolute values are similar for the two interface types and for the two nanocapacitors. They also provide a simple way of recovering the values introduced in the FEM simulations and shown Figure 4d from which the slopes given in Tables 1 and 2 were calculated. E.g., if we consider the HfO_2/Al_2O_3 interface for the nanocapacitor A with a total thickness of 66 nm and an applied voltage of 6 V, the charge density σ_{A2} is equal to 0.85 μC cm^{-2}, a value slightly higher than 0.78 μC cm^{-2} measured by FEM and represented Figure 4d. The discrepancy comes from the effective electric field taking into account screening by the charged layers at the metal/dielectric interfaces and the potential loss ΔV as discussed in the previous section. We notice for instance that the free trapped charge densities are slightly lower for B than for A (for a given applied field), which is caused by the slightly weaker effective electric field in B than in A, as pointed out previously, due to the greater screening provided by the trapped charges at the interfaces with the electrodes.

These equations also suggest that the charge trapping between the dielectrics is controlled by their difference in permittivity and the average electric field, which explains why the nanocapacitor B, with different stacking sequences of HfO_2 and Al_2O_3 dielectrics, also has an electric field distribution equiv. to that of the nanocapacitor A. The homogenization of the electric field implies that the density of free trapped charges has to correspond to the density of the polarization charges at the dielectric/dielectric interfaces induced by the bias. As mentioned above, the charged interfacial layers are located in the chemical transitioning region of the dielectric/dielectric interfaces, whatever the stacking order is. However, this raises the question of the specific role of the chemical defects that are certainly present at these interfaces, since reversible oxygen migration or defect redistribution may be favored upon the applied electric field.[73] It is worth asking whether the same results would be obtained or not with a different density value of defects or even in the absence of these defects.

Besides the charged interfacial layers for both A and B, free charges are also present at the electrodes and depend on the applied bias. The slope extracted from their bias dependence, determined from the best agreement between FEM modeling and experimental phase profiles, are 0.43 ± 0.05 and -0.74 ± 0.05 μC cm^{-2} V^{-1} for A at the top and bottom electrodes respectively, and 0.30 ± 0.05 and −0.49 ± 0.05 μC cm^{-2} V^{-1} for B.

A last comment can be made about the origin of the charges trapped at the interfaces between the dielectrics. Nanocapacitors are never perfect capacitors, as they exhibit leakage currents that have to be taken into account under DC bias. The electric currents of A and B measured during the operando holography experiment are presented in the Supporting Information (see Figures S12 and S13, Supporting Information). We deduced a very low electrical conductivity, which never exceeds 0.1 S m^{-1} and 0.3 S m^{-1} for A and B, respectively, even for the highest bias up to 12 V for A. The potential loss ΔV determined by the FEM modeling increases with the applied bias and follows the leakage current variation suggesting that there is a series of resistance (or contact resistance) in the circuit.[74] It is therefore possible that some of the charge carriers participating in the leakage current are trapped at the uncompensated dielectric/dielectric interfaces, and then released from the traps before being replaced by new incoming charges. This trapping/de-trapping mechanism under a DC bias and for a significant period of time is equiv. to a static equilibrium in the charge distribution as we observe it. It would be, therefore, particularly interesting to access the dynamics of this process using time-resolved experiments during charging/discharging cycles.

4. Conclusions

We studied twin trilayer nanocapacitors, $HfO_2/Al_2O_3/HfO_2$ (A) and $Al_2O_3/HfO_2/Al_2O_3$ (B) with TiN electrodes using operando electron holography experiments. In combination with FEM simulation, we evidenced the presence of negative or positive trapped charges at different interfaces (dielectric in contact with a metal and dielectric in contact with a dielectric) upon biasing and further quantitatively clarify the influence of these interfacial layers on the electric field distribution.

In contrast to the theoretical calculation for perfect capacitors composed of dielectrics with different permittivities, an equiv. electric field distribution throughout the whole dielectric stack is observed. The presence of trapped charges at the dielectric/dielectric interfaces leads to the uniformization of the electric field distribution inside the trilayer dielectric stack. The charges at the metal/dielectric interfaces screen the applied field so that the effective field across the dielectrics is lower. After quantification of the equiv. surface charge densities at the different interfaces, we found a linear relationship with the applied bias for all of them. The trapped charge densities at the metal/dielectric interfaces depend on the stacking sequence (leading to different interfacial layers in terms of defects due to different processing), the nature of the dielectric and the sign of the bias. The bias dependence of the interfacial charges is similar for the HfO_2/Al_2O_3 and Al_2O_3/HfO_2 interfaces, but the sign of the charge trapped is opposite as expected: negative for Al_2O_3/HfO_2 and positive for HfO_2/Al_2O_3 when the bias is applied on the top electrode. The amount of charge trapped at these dielectric/dielectric interfaces is related to the difference in permittivity to homogenize the effective field. This may be the driving force for explaining the presence of the charges trapped on the dielectric/dielectric interfacial layers. It would be interesting to study other systems of the same type to investigate if this result could be generalized to all interfaces between dielectrics of different permittivities.

Thanks to a setup and a methodology improving the sensitivity, associated with a high spatial resolution, the information gained with operando electron holography on the location of the trapped charges, their densities, and the associated electric field distribution provide unique insights on the behavior of nanocapacitors. Operando electron holography is a powerful technique that can be applied to any dielectric stacks, including ferroelectric ones, to understand and optimize device functionality and performance.

Its ability to determine the internal electric field over a large field of view and to quantify the trapped charge densities at each of the interfaces in a heterostructure opens avenues for designing proper interfaces to optimize a large variety of nanoelectronics, optoelectronics, and photovoltaics devices.

Another interesting outlook would be to access the dynamic of the trapping/detrapping processes using time-resolved experiments during charging/discharging cycles.

5. Experimental Section

Heterostructure Preparation: The metal-insulator-metal (MIM) capacitors (A and B) were fabricated on *p*++ Si substrates (*p*++, 10^{18} atoms·cm^{-3}). Prior to the deposition, the Si wafers were cleaned with a standard SC1 solution (SC1: 10 min, 70–80 °C, (5:1:1) $H_2O + NH_4OH$ (29% weight) + H_2O_2 (30% in solution)) followed by HF dip (HF 1%, 15 s) to remove native SiO_2 from the wafer surfaces. The 30 nm thick TiN bottom electrode was sputter-deposited at room temperature. Then, HfO_2 and Al_2O_3 films were deposited by atomic layer deposition (ALD) using an "Oxford FlexAl" system at 250 °C. Tetrakis(ethylmethylamino)hafnium (TEMA-Hf) and trimethylaluminum (TMA) were used as metal sources for HfO_2 and Al_2O_3, respectively. Water was used as an oxidant for both ALD processes. The TiN top electrode with a thickness of 30 nm was deposited again by sputtering at room temperature. For macro capacitor devices, the TiN top layer was patterned into square pads of 95 × 95 µm^2 area by photolithography and liftoff of a Ti (30 nm)/Au (100 nm) bilayer followed by etching using a SC1 solution at 50 °C.

FIB-Assisted Sample or Specimen Device Preparation: Standard cross-section thin lamellas were prepared by Ga^+ source FIB (Helios 600i from FEI) for TEM/STEM characterizations. The lift-out method process consists of depositing a protective Pt layer, cutting the slice perpendicular to the surface, lifting-out of the slice with the micromanipulator, mounting the specimen to a supporting Cu grid, and finally polishing the lamella to the desired dimensions and thicknesses. Dedicated FIB specimen preparation[74,75] is key to operando electrical biasing TEM experiments, for which a lamella device is constructed and adapted on a commercialized Hummingbird chip compatible with biasing holder (1 600 series, Hummingbird scientific). The architecture of the chip is shown in Figure S1a (Supporting Information). It has nine conductive, separate Au tracks (as labeled from No. 1 to 9), which are perfectly compatible with the nine separate Au contacts in the dedicated biasing sample holder (1 600 series, Hummingbird Scientific). The local magnification image of the chip (see Figure S1a, Supporting Information) shows its working window, in which the FIB-prepared lamellae are placed between two electrodes of the Hummingbird chip. In practice, the lift-out of the chunk was performed at a stage tilting angle of 52° with the aid of the micromanipulator; and, subsequently, the chunk was mounted between two Au pads (3 and 7). During the lift-out procedures, gas injection system (GIS) was used to create Pt deposition between the contacts. The next step was to make some undercuts to avoid the leakage current from electrical circuit pathways (Si substrate or Pt layer). Then, the chunk was thinned to a thickness of ≈50–60 nm, with the milling voltage gradually decreasing from 30 to 5 kV. The specimen preparation was finished with a cleaning at low energy (1–2 kV) to minimize damaged layers on the surfaces. The Hummingbird biasing sample holder with the inserted chip is illustrated in Figure S1b (Supporting Information). At the back of the sample holder are connected cables allowing electrical signal input from the source generator. The specific architecture and the fabricated specimen devices of A and B are displayed in Figure S2 (Supporting Information).

TEM Experiments: The bright field (BF)-STEM and high angle annular dark field (HAADF)-STEM images and STEM-EELS measurements were performed using a JEOL JEM-ARM200F microscope with a 200 kV accelerating voltage and equipped with a probe aberration corrector (ASCOR from CEOS). EELS acquisition was performed by a Gatan GIF Quantum ER imaging filter equipped with a model 994 UltraScan 1000XP Gatan camera. EELS 2D spectrum was recorded with an entrance aperture of 5 mm and a wide dispersion of 1 eV/channel, allowing simultaneous acquisition of Hf-$M_{4,5}$, Al-K, Ti-$L_{2,3}$, N-K, and O-K edges in the core-loss spectrum ranging from 300 to 2348 eV, and the energy resolution is ≈3 eV. EELS 2D spectrum was also acquired with a dispersion of 0.25 eV/channel and an entrance aperture of 2.5 mm, enabling an energy resolution of ≈1.5 eV. The step size is 0.13–0.25 nm and the sample drift is ≈0.25 nm during the acquisition time (≈2 min), giving an error bar of 0.4–0.5 nm.

Operando electron holography experiments were performed on the I2TEM microscope, a Hitachi HF3300-C TEM, specially designed for in situ electron interferometry experiments. The microscope was equipped with a cold field-emission gun (CFEG) for optimal brightness, a double stage configuration consisting of an upper stage positioned above the objective lens to allow the specimen to be observed in field-free conditions (Lorentz mode), and a conventional stage between the pole-pieces of objective lens (normal mode). The aberration corrector (BCOR from CEOS) allows a large field of view and spatial resolution of 0.5 nm for the Lorentz mode.[76]

Holography experiments were performed at an operating voltage of 300 kV ($C_E = 6.53 \times 10^6$ V^{-1} m^{-1}), Lorentz stage, elliptical illumination and two post-specimen biprisms to allow flexibility in the holographic configurations and to eliminate the Fresnel fringe artifacts.[77] The Lorentz mode was chosen to accommodate a sufficiently large field of view that encompassed the substrate, dielectric, top electrode, and vacuum. Holograms were recorded using a Gatan© K3 camera functioning at a rate of 1 or 2 frames per second (fps). The interfringe was set at 0.45 nm (6.5 pixels) and the hologram acquisition was performed using dynamic automation and the pi-shift method[78] over a total exposure time of 120 s thanks to different software specifically developed: FringeControl for feedback control of the holographic fringes, Specimen Control for the specimen drift compensation (real time stage correction) and a specific process for the image acquisition. All routines are individual and independent processes. The software ran on the same computer used to control the camera. In-house scripts and dedicated code implemented within Digital Micrograph for GMS 3.3 (Gatan Inc.) were used to analyze the holograms and extract amplitude and phase images during post-processing. With this setup (I2TEM and K3 camera) combined with dynamic automation, the resulting phase noise after all data treatment processes is lower than 10 mrad when the phase profile across the layers is integrated at 120 nm.

Electrical Measurements: Electrical biasing and measurements during operando electron holography experiments were carried out with a Keithley 4200A-SCS instrument with 2 4225-PMU, SMU, CVU, and 2 RPM remote amplifier modules. The DC biasing was provided by a Keithley 2635B source meter. The capacitance versus voltage measurements of the 95 × 95 µm^2 capacitors were performed at 100 kHz using a Keysight B1500A analyzer on an MPI TS2000-SE probe station.

FEM Simulation: FEM simulations were conducted in a 2D geometry using COMSOL Multiphysics 5.6, a software specifically designed for studying the physical properties of systems, particularly those involving coupled physics problems. The stationary solver was applied to address the electrical distribution inside and outside the sample.

The modeled region was square, 3.5 µm in both the propagation direction of the fast electron and the direction perpendicular to the interfaces, as shown in Figure S14 (Supporting Information). Not only the specimen geometry (e.g., the lamella thickness, the length of each layer, the width of top and bottom electrodes) and the relative permittivity values, but also the charging layers at interfaces were incorporated into the models. The model geometry was determined using the amplitude image reconstructed from the electron hologram. Regions of different mesh sizes were used to improve the efficiency of the calculations to create a model that sufficiently encompassed the active region and surrounding vacuum. The triangular mesh evolved in size from the external boundaries to the active area, from a maximum of 0.4 µm to a minimum of 0.4 nm in the area around the dielectric layer. These values of mesh size represent the straight-line distance between neighboring nodes. Since these nodes are not on a cubic mesh, the spatial resolution of the simulated projected potential is smaller than these values. The whole model was surrounded by a layer that approximates an extension of the equations to infinity. The bottom electrode and model boundaries were grounded and a fixed potential

applied to the top electrode. The electrostatic potential was calculated and integrated into the propagation direction to simulate the phase change of the fast electron according to Equation 1 in the main text. The width and volume charge density of each interfacial charged layer was adjusted until the best agreement with the experimental phase profiles was obtained.

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

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Conflict of Interest

The authors declare no conflict of interest.

Author Contributions

CG, MH, and CD initiated and supervised the study. MHR grew the samples and RW performed the macroscopic electrical measurements under the supervision of CD. CG and LZ designed and developed the experimental procedure, LZ prepared the in situ TEM samples and assisted CG in performing the in situ experiments. LZ prepared the TEM/STEM samples and performed the experiments. CG and LZ processed the electron holography data. LZ performed all the FEM modeling and the figures. CG, LZ, KG, and MJH interpreted holography results and FEM modeling. CG, LZ, KG, MJH, and CD discussed the results. LZ and CG wrote the first draft of the paper further edited by MJH and CD. All authors contributed to the correction of the manuscript.

Data Availability Statement

The data that support the findings of this study are available from the corresponding author upon reasonable request.

Keywords

Al_2O_3, HfO_2, interface charge trapping, interfacial layers, nanocapacitor, operando electron holography

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