Development of ferroelectric tunnel junction devices based on hafnia zirconia films for neuromorphic applications

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Declaration of authorship

I hereby declare that I alone am responsible for the content of my doctoral dissertation and that I have only used the sources or references cited in the dissertation.

Date: 15.07.2024 Keerthana Shajil Nair

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Abstract

This thesis focuses on the development of FTJ devices using a $Hf_{0.5}Zr_{0.5}O_2$ (HZO) ferroelectric layer, demonstrating their compatibility with CMOS integration and their applicability in neuromorphic hardware. A bilayer structure comprising metal- ferroelectric-dielectric-metal layers with a $\sim$ 10 nm HZO ferroelectric layer and a thin tunneling Al_2O_3 layer has been investigated.

We examine the impact of dielectric positioning, metal electrode placement (with W and TiN), and dielectric thickness on device performance. Additionally, we explore the role of charge traps in the dielectric or at the dielectric-ferroelectric interface, and the influence of the fabrication process on charge trap density and polarization switching behavior. W bottom electrode is found to give optimized device performance, and positioning Al_2O_3 next to the bottom electrode further enhances the device performance in terms of ON current and ON/OFF ratio. Furthermore, longer pulses are necessary to stabilize higher remnant polarization due to charge trap dynamics.

We also analyze various electrical parameters affecting FTJ device performance, demonstrating that the cycling waveform significantly influences the wake-up process and the resulting remnant polarization in TiN-Al_2O_3-HZO-W FTJ devices. Square waveforms outperform triangular waveforms, yielding higher remnant polarization (P_R) post-wake-up. By employing an asymmetric waveform for field cycling and adjusting the pulse width, the P_R and the ON/OFF ratio after wake-up are significantly improved.

Finally, we explore the integration of bilayer FTJ devices into CMOS back-end-of-line (BEOL) processes, demonstrating a 1T1C circuit by connecting an FTJ in the BEOL with an nMOS transistor in the front-end-of-line. Measurements on standalone FTJ devices in the BEOL reveal an ON/OFF ratio of 18 and an ON current density of 24.5 $\mu A/cm^2$. Crucially, BEOL fabrication has negligible impact on transistor characteristics, and the 1T1C circuit exhibits a 2.6-fold amplification of the FTJ ON current. The FTJ devices integrated on the CMOS-BEOL demonstrate multiple resistance states with the application of partial switching Reset and Set pulses. These FTJ devices have the potential to be utilized in neuromorphic hardware systems.

Zusammenfassung

Diese Arbeit konzentriert sich auf die Entwicklung von FTJ-Bauelementen unter Verwendung einer ferroelektrischen $Hf_{0,5}Zr_{0,5}O_2$ (HZO)- Schicht und demonstriert sowohl die CMOS- Integrierbarkeit der Bauteile als auch deren Anwendbarkeit für neuromorphe Hardware. Hinsichtlich dieser Aufgabe wurden Doppelschichtstrukturen bestehend aus Metall-Ferroelektrikum-Dielektrikum-Metall-Schichten, mit einer $\sim$ 10 nm großen ferroelektrischen HZO-Schicht und einer dünnen Al_2O_3 Tunnelschicht, untersucht.

Wir erforschten unter anderem die Auswirkungen der Positionierung des Dielektrikums, der Platzierung der Metallelektroden (jeweils aus W und TiN) und auch der Dicke des Dielektrikums hinsichtlich auf der Bauelement- Leistung. Außerdem studierten wir die Rolle von sogenannten Ladungsfallen im Dielektrikum und/oder an der dielektrisch-ferroelektrischen Grenzfläche, sowie den Einfluss des Herstellungsprozesses auf die Ladungsfallendichte und das Polarisationsschaltverhalten. Zuerst konnte gezeigt werden, dass die W-Bodenelektrode eine optimierte Bauelementleistung bietet. Ebenso verbesserte die direkte Positionierung von Al_2O_3 neben der Bodenelektrode die Bauelementleistung hinsichtlich des "ON current" und des "ON/OFF"- Verhältnisses. Wir beobachteten zudem, dass längere Pulse erforderlich sind, um eine höhere Restpolarisation aufgrund von Ladungsfallendynamiken zu stabilisieren.

Im nächsten Schritt analysierten wir verschiedene elektrische Parameter, die die Leistung von FTJ- Bauelementen beeinflussen, und zeigten, dass die zyklische Wellenform den sogenannten Aufwachprozess und die daraus resultierende Restpolarisation in TiN-Al_2O_3-HZO-W FTJ-Bauelementen erheblich beeinflusst. Rechteckige Wellenformen übertreffen dreieckige Wellenformen und führen zu einer höheren Restpolarisation nach dem Aufwachen. Durch die Verwendung einer asymmetrischen Wellenform für den Feldzyklus und die Anpassung der Pulsbreite wurde die Restpolarisation und das ON/OFF-Verhältnis nach dem Aufwachprozess deutlich verbessert.

Schließlich demonstrierten wir die Integration von zweischichtigen FTJ-Bauelementen im CMOS-Back-End-of-Line (BEOL)-Prozess mit Hilfe einer 1T1C-Schaltung, indem wir einen FTJ im BEOL mit einem nMOS-Transistor im Front-End-of-Line verbanden. Messungen an eigenständigen FTJ-Bauelementen im BEOL ergaben ein ON/OFF-

Verhältnis von 18 und eine ON-Stromdichte von 24,5 $\mu\mathrm{A}/\mathrm{cm}^2$. Entscheidend ist, dass die BEOL-Fertigung vernachlässigbare Auswirkungen auf die Transistoreigenschaften hat und die 1T1C-Schaltung eine 2,6-fache Verstärkung des FTJ- On-Currents aufweist. Die auf dem CMOS-BEOL integrierten FTJ-Bauelemente zeigen zudem mehrere Widerstandszustände bei der Anwendung von partiellen Reset- und Set-Pulsen. Diese FTJ-Bauelemente haben daher das Potenzial, in neuromorphen Hardwaresystemen eingesetzt zu werden.

Introduction

Memory devices are one of the key components of computing systems. It is a necessary part of almost every digital computing system, enabling the execution of software applications and the preservation of user data.

The demand for advanced memory solutions has grown significantly due to the rapid integration of technology into daily life, mainly through the internet of things (IoT). Hence, there is a need for innovations that offer high storage density, fast operations, low power consumption, and cost-effectiveness. While existing memory technologies like static random access memory (SRAM), dynamic random access memory (DRAM) and flash memory have driven the evolution of digital devices, they face significant limitations that challenge their suitability for future demands. SRAM and DRAM are utilized for fast access but are volatile. Hence they are limited to data storage during computations. A single SRAM cell consists of several transistors (typically six), which results in a larger SRAM size compared to DRAM. This larger size results in lower storage density and can limit the scalability [1]. DRAM, being volatile, requires constant power to maintain data, leading to high energy consumption [2, 3]. For long-term data storage, the main memory technology in use is Flash memory owing to its non-volatility. However, flash suffers from slow write and limited endurance [4, 5]. Furthermore, flash device process technology is not compatible with advanced Complementary Metal-Oxide-Semiconductor (CMOS) technology on which digital processors are fabricated. Therefore, new non-volatile memory technologies are being developed, as shown in Figure 1 to enable on-chip memory for emerging data intensive applications.

In recent years, the use of artificial intelligence in various aspects of human lives has increased significantly. Applications such as facial recognition, image recognition, pattern classification, autonomous vehicles, and robotics are just a few examples [6–8]. While these tasks are currently executed on digital CMOS computational platforms, the data-heavy applications anticipated in the future necessitate hardware that can make autonomous decisions [9]. This highlights the need to move beyond the traditional von-Neumann computational architecture, which involve extensive data transfers between the central processing units (CPUs) and main memory. This constant data exchange elevates

power consumption and prolonged data processing duration which is collectively referred as the Von-Neumann bottleneck [10].

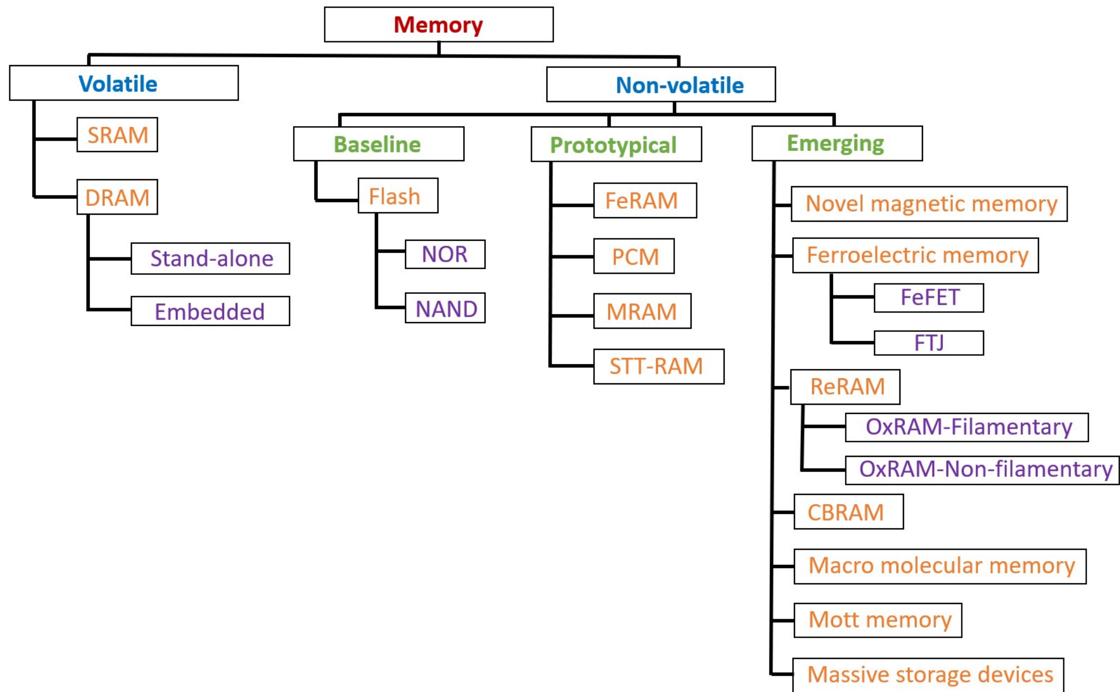

Figure 1: Schematic overview of the memory technology landscape. A classification of memory types showing the hierarchy of volatile and non-volatile memory technologies. Volatile memories include SRAM and DRAM, which are further divided into stand-alone and embedded types. Non-volatile memories are categorized into baseline (Flash, NOR, NAND), prototypical (FeRAM, PCM, MRAM, STT-RAM), and emerging technologies. Emerging non-volatile memories include novel magnetic memory, ferroelectric memory (with FeFET and FTJ), ReRAM (with OxRAM filamentary and non-filamentary), CBRAM, macro molecular memory, Mott memory, and massive storage devices. Figure reproduced from [11].

Neuromorphic computing represents a paradigm shift in the computational technology, inspired by the architecture of the human brain [12,13]. This approach to computing involves the design of electronic systems that mimic the brain's structure and processing methods, aiming to achieve the efficiency and adaptability of the biological neural networks [10]. Neuromorphic systems utilize specialized hardware, such as artificial neurons and synapses, which allow them to process information in a highly parallel and energy-efficient manner. The neural networks can be classified into two groups namely, artificial neural networks (ANN) and spiking neural networks (SNN). The ANN processes information using layers of neurons that activate continuously and are typically trained with methods like backpropagation [14, 15]. Backpropagation is an algorithm used to train

ANNs by iteratively adjusting weights to minimize the error between the predicted and actual outputs. In contrast, SNN mimics biological brain activity more closely, using discrete spikes (electrical pulses) to communicate between neurons and incorporating the timing of these spikes into their computation. SNNs often utilize unique learning rules such as spike-timing-dependent plasticity (STDP) and are known for their energy efficiency [16]. Emerging memory devices that mimic the functionality of biological synapses and neurons can be used as neuromorphic hardware components [9]. The requirements for such memories are as follows,

- Ability to program the conductance in analog fashion
- Low-voltage operation
- Fast switching
- Possibility to scale the devices for dense integration.

Figure 2 illustrates the emerging memory devices that have shown potential to be used as components in neuromorphic hardware systems. Filamentary memristors, phase change memories (PCM), and ferroelectric tunnel junctions (FTJ) are 2-terminal devices. However, ferroelectric transistors, electrochemical transistors, and charge-trapping transistors are 3-terminal devices. Even though these devices have successfully demonstrated functions of neurons or synapses as proof of concept [10, 17–21], the large scale implementation needed for real world applications requires them to be compatible with CMOS technology [9]. For ferroelectric RAM, the technology used hitherto was based on ferroelectric perovskite materials. However, these could not be scaled to low dimensions limiting their integration in advanced CMOS technology. The discovery of ferroelectricity in Hafnium oxide (HfO_2) [22] brought a solution to the scalability issue faced by conventional perovskite based ferroelectric materials and HfO_2 is widely used as a high-k dielectric material in CMOS processes, particularly for gate oxides in transistors [23]. The ease of integration with existing CMOS technology has increased interest in hafnium-based ferroelectric memory devices.

Ferroelectric materials exhibit spontaneous electric polarization that can be reversed by an external electric field, providing a mechanism for non-volatile memory that does

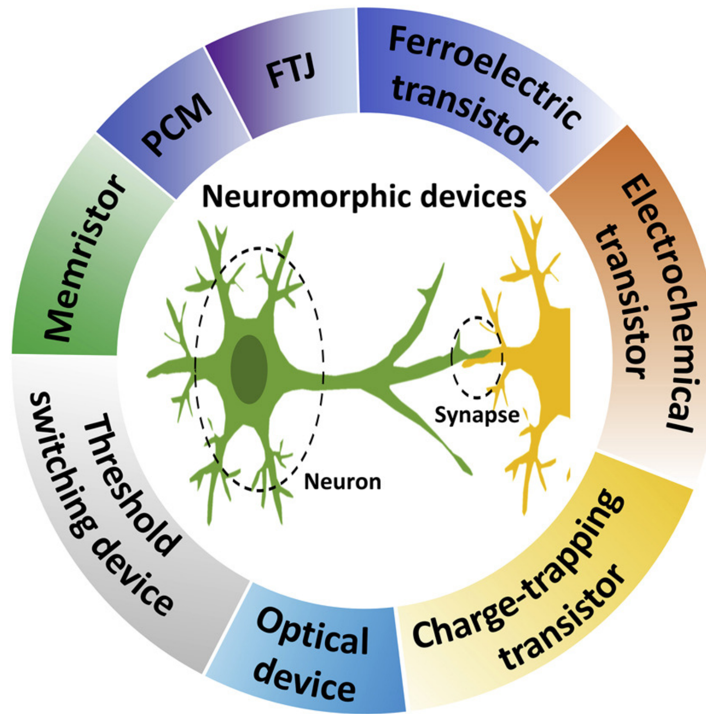

Figure 2: Emerging memory devices for neuromorphic applications. Figure reproduced from [10].

not require power to maintain data state. As polarization switching is an electric-field driven phenomena (with only displacement current flowing), low power consumption can be achieved during memory write/erase operations. This characteristic makes ferroelectric memories particularly attractive for energy-sensitive applications such as wearable technology and IoT devices. FTJs leverage these properties to create memory devices that offer not only reduced power consumption but also the potential for high-density integration due to its reduced footprint from 2-terminal architecture. Additionally, FTJs support multi-level data storage which is essential for neuromorphic applications. By using HfO_2 based ferroelectric layer, they become CMOS compatible and with a possible reduction in the processing temperature to $\leq$450 °C, they can even be integrated to the back-end-of-line (BEOL) of CMOS technology [23].

This doctoral thesis addresses the need for advanced on-chip non-volatile memory technologies by exploring FTJ devices based on a $Hf_{0.5}Zr_{0.5}O_2$ (HZO) ferroelectric layer. The research focuses on metal-ferroelectric-dielectric-metal (M-FE-DE-M) FTJ devices,

which utilize a thicker ferroelectric layer (approximately 10 nm) while maintaining a high ON current and ON/OFF ratio. Tungsten (W) and Titanium Nitride (TiN) metals are selected as the electrodes for the M-FE-DE-M FTJ devices due to their compatibility with CMOS technology. The chosen HZO crystallization temperature of 400°C ensures that these devices are CMOS-BEOL compatible. Recognizing the significant impact of interface quality on the performance of tunnel junction devices, this work commences with the optimization of the M-FE-DE-M FTJ device architecture. This involves a detailed investigation into the effects of dielectric and metal electrode positioning to enhance device performance. Subsequently, this study examines the influence of dielectric thickness on the properties of the FTJ devices. Additionally, this research explores various fabrication process flows to determine their impact on device performance, aiming to optimize the fabrication process for these FTJ devices.

This work aims to investigate the wake-up effect observed in the HZO ferroelectric layer, where polarization increases with electric field cycling, as seen in FTJ devices based on HZO layers. The objective is to study the role of field cycling operations on FTJ device properties by utilizing different waveforms for field cycling. Optimizing the cycling waveform is expected to achieve the highest remnant polarization (P_R) and ON/OFF ratio from a given FTJ stack. Additionally, the research seeks to modify electrical parameters of Reset and Set pulses to enable partial polarization switching in the ferroelectric layer, thereby demonstrating multiple resistance states in the FTJ devices. These multiple resistance states are crucial for neuromorphic applications, and achieving this in the devices is a primary objective of this study.

This research seeks to demonstrate the CMOS-BEOL integration of optimized FTJ devices and characterize their properties using optimized electrical parameters. Additionally, it seeks to study the impact of FTJ integration on CMOS front-end transistors by analyzing their properties before and after the integration process. Furthermore, the research aims to utilize front-end nMOS transistors to amplify the read currents from the FTJ devices through a 1T1C circuit configuration.

This work has been carried out and partly funded in the framework of the Horizon 2020 European project "BEOL Technology Platform based on Ferroelectric Synaptic Devices for Advanced Neuromorphic Processors" (BeFerroSynaptic - (no. 871737)). This

EU project (January 2020 - December 2023) was coordinated by Dr. Stefan Slesazeck from NamLab GmbH in Dresden. The objective of this project was to develop advanced neuromorphic processors by integrating ferroelectric synaptic devices such as FTJs and FeFETs into CMOS technology, enhancing device performance, and demonstrating practical applications in AI and edge computing, thereby significantly reducing power consumption and improving efficiency.

Organization of this thesis

This thesis is structured into five chapters, each addressing different aspects of FTJ memory devices for neuromorphic applications.

In Chapter 1, we present the scientific background and a comprehensive literature review. It covers the fundamental properties and various types of ferroelectric materials, with a focus on hafnium-oxide-based ferroelectric thin films. The chapter explores the application of ferroelectricity in memory devices, polarization switching mechanisms, and the physics of FTJ devices. It also delves into charge transport mechanisms in FTJs, the M-FE-DE-M device architecture for FTJs, and the application of FTJs in neuromorphic computing.

In Chapter 2, we detail the methods used for fabricating and characterizing the FTJ devices. This includes material deposition techniques, lithography methods, thickness and chemical analysis methods, the device fabrication process flow, and various electrical characterization techniques. Additionally, the characterization of M-FE-M capacitor structures is also presented.

In Chapter 3, we investigate the bilayer structure (M-FE-DE-M) of FTJ devices, focusing on the effects of dielectric positioning, metal electrode positioning, dielectric thickness, sample fabrication process flows, and the significance of charge traps within the FTJ stack.

In Chapter 4, we analyze the impact of various electrical parameters on FTJ device performance. This includes examining the effects of cycling waveforms on the wake-up behaviour and ON/OFF ratio of the FTJ devices, as well as utilizing modified Reset and Set pulses to achieve multiple resistance states in the FTJ devices.

In Chapter 5, we explore the integration of optimized FTJ devices with CMOS-BEOL,

detailing the fabrication process flow for CMOS integration of FTJs. Stand-alone FTJ and front-end transistor measurements are performed to characterize the components individually. Subsequently, the FTJ devices are connected to the front-end transistors to create a 1T1C circuit configuration, which is used to amplify the read currents from the FTJ. The results of these experiments are presented in this chapter.

Finally, we summarize the key findings of our research, highlighting the contributions and implications of the study and suggest potential future research directions to further advance the field of FTJ memory devices for neuromorphic applications.

Chapter 1

Scientific background

1.1 Ferroelectricity

The term ”ferroelectricity” is similar to ”ferromagnetism” in magnets, where materials exhibit a permanent magnetic moment. However, in ferroelectric materials, this concept applies to electric polarization instead of magnetism. Ferroelectricity is a property shown by certain materials that exhibit a spontaneous electric polarization. These materials can maintain an electric dipole moment even in the absence of an external electric field. This exhibited polarization is not fixed and can be reversed by the application of an external electric field. The ability to switch the direction of polarization supports many of the practical applications of ferroelectric materials. Key characteristics of ferroelectric materials include:

- **Spontaneous Polarization:** The natural ability of the material to form a dipole moment.
- **Switchable Polarization:** The direction of the polarization can be switched or reversed by applying an external electric field.
- **Hysteresis Loop:** When the polarization as a function of the electric field is plotted, ferroelectric materials show a hysteresis loop, similar to ferromagnetic materials. This property is useful for memory storage devices, as the state of the polarization (up or down) can represent binary information.

1.1.1 Fundamental properties

Dielectrics are insulating materials that do not conduct electricity but can support electric fields, which allows them to store electrical energy. Within this category fall the piezoelectrics, materials that generate an electric charge in response to mechanical stress. Piezoelectrics further include a subset known as pyroelectrics, which generate an electric charge when the temperature is varied. Ferroelectric materials are a specialized group within pyroelectrics, characterized by their ability to retain their electric polarization after an external electric field is removed. Each category represents a progressively specific type of behaviour related to the material's interaction with electrical and mechanical forces [24]. This classification is schematically shown in Figure 1.1.

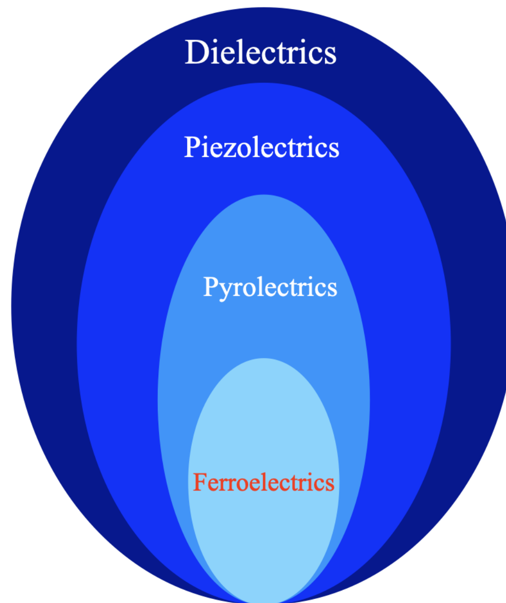

Figure 1.1: Pictorial representation of various subgroups of dielectric materials.

In a ferroelectric material, the electric displacement (D) is defined as

$$\mathrm{D} = \epsilon_0 \mathrm{E} + \mathrm{P} \tag{1.1}$$

where ϵ_0, E and P are the vacuum permittivity, electric field, and polarization, respectively. This polarization can be expressed in terms of the spontaneous polarization ($\mathrm{P_S}$) and the linear dielectric response as follows

$$\mathrm{P} = \epsilon_0 \chi \mathrm{E} + \mathrm{P_S}, \tag{1.2}$$

where χ is the electrical susceptibility of the medium. A linear dielectric shows a linear polarization response to the applied electric filed. However, ferroelectric material shows a hysteresis loop as shown in Figure 1.2(a) in response to the applied electric filed. The Y-axis intercepts in the positive and negative sides are the positive and negative remnant polarization ($\mathrm{P_R}$) values. It is the residual polarization that remains in a ferroelectric material after the external electric field is removed. The X-axis intercepts in the positive and negative sides are the coercive field ($\mathrm{E_C}$) values. It represents the external electric field that must be applied to a material to reduce its polarization to zero from the remnant value. The Curie temperature ($\mathrm{T_C}$) of a ferroelectric material is the temperature above which the material loses its ferroelectric properties and becomes paraelectric. At temperatures below the T_C, the material exhibits spontaneous electric polarization.

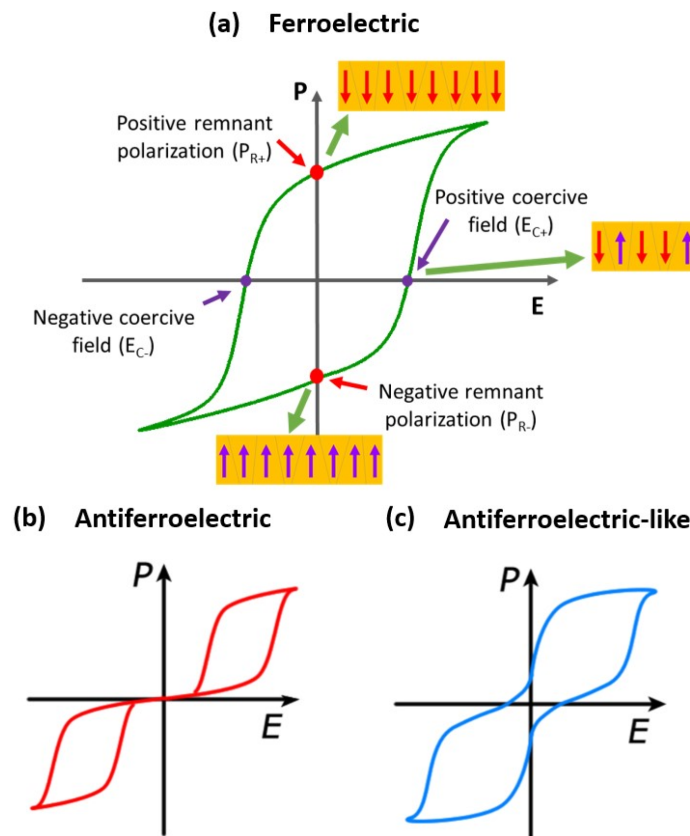

Figure 1.2: Schematic showing three types of electrical polarization responses to applied electric fields: (a) A single loop typical of ferroelectrics; (b) A double hysteresis loop with zero remnant polarization, typical of antiferroelectric (AFE) state; (c) A pinched hysteresis loop with small but noticeable remnant polarization. We call this an antiferroelectric-like state. The figures (b) and (c) are adapted from [25]. The domain orientations for different polarization states are shown in the inset of (a).

The ferroelectric material has a non-centrosymmetric crystal structure, resulting in a non-centrosymmetric distribution of charges in the unit cell. This results in the formation of the dipole with a dipole moment p. The macroscopic polarization P is the sum of individual dipole moments normalized by the volume of the unit cell. Although charges are balanced within the bulk of the material, there are unbalanced charges at the surface of the solid. Therefore, polarization can also be described in terms of surface charge, and it shares the same units as charge density. The regions within a material where the electric dipoles are aligned in a uniform direction are known as the domains (shown in Figure 1.2(a)). These domains form as a result of the minimization of the material's free energy. In a single-domain ferroelectric, the coercive field is represented by a single value. However, in a ferroelectric material with multiple domains, each domain may possess a distinct coercive field. This variability leads to a distribution of coercive fields, which causes a tilt in the ferroelectric hysteresis loop.

When there are several domains in the material and the adjacent dipoles are oriented in anti-parallel configurations, this might lead to a net zero polarization in the absence of an external electric field. Such a state is known as an antiferroelectric state. This state gives a double hysteresis loop as polarization response to the external electric field, see Figure 1.2(b). When there is a coexistence of both ferroelectric and antiferroelectric regions, the material shows a pinched hysteresis loop as shown in Figure 1.2(c). This type of hysteresis loop is referred to as an antiferroelectric-like hysteresis loop [25].

Ferroelectricity and antiferroelectricity are phenomena associated with the spontaneous alignment of electric dipoles within a material, which can be described using the Landau-Ginzburg formalism. This formalism is a thermodynamic approach that leverages the concept of order parameters to describe phase transitions, including those in ferroelectrics and antiferroelectrics [26, 27]. Ferroelectricity is characterized by a uniform alignment of electric dipoles in the same direction, which can be modelled using a single order parameter representing the polarization magnitude and direction. The Landau-Ginzburg theory for ferroelectricity involves a free energy expansion in terms of the polarization order parameter, where the stability and change of phases can be influenced by temperature, electric field, and mechanical stress. Antiferroelectricity, on the other hand, involves a more complex arrangement where adjacent dipoles are oriented in

opposite directions, leading to a cancellation of the overall polarization. This requires a multicomponent order parameter that can describe the relative orientations of the dipoles.

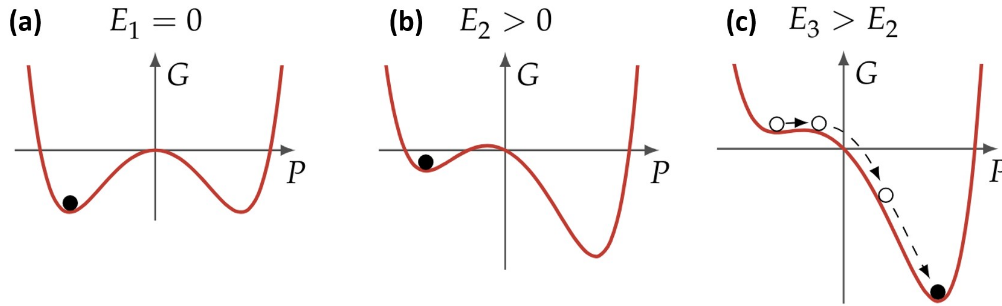

Figure 1.3: (a) Gibbs free energy potential (G) in the absence of external field (E). (b) Asymmetric potential landscape under the influence of non-zero electric field. (c) Destabilization of one polarization state by the application of a higher electric field, leading to switching of polarization. [Reproduced from [28]]

In a simple *uniaxial* ferroelectric[1], the polarization can exist in two stable states, which correspond to the two polarization directions (+P and -P). In the absence of an external field, there is no energy difference between these two states. The Gibbs free energy (G) of the ferroelectric material can be described as,

$$\mathrm{G} = -\mathrm{EP} + \frac{\alpha}{2}\mathrm{P}^2 + \frac{\beta}{4}\mathrm{P}^4 + \frac{\gamma}{6}\mathrm{P}^6 + \ldots, \tag{1.3}$$

where α, β and γ are the Landau coefficients which control the order of the phase transition. Generally, it is not necessary to consider orders of P higher than six. The term $-\mathrm{EP}$ accounts for the contribution from the external electric field. Application of a positive (negative) electric field reduces the Gibbs free energy of the positive (negative) polarization. A stable state is achieved by minimizing G. This mechanism explains how polarization is switched by applying an external electric field, as illustrated in Figure 1.3.

1.1.2 Different types of ferroelectric materials

Historically, the concept of ferroelectricity dates back to 1912 when Erwin Schrödinger first proposed the term [29, 30]. However, the first actual discovery of ferroelectricity occurred in 1921 with Rochelle salt ($NaKC_4H_4O_6{\cdot}4H_2O$) [31]. The instability against

[1] Uniaxial ferroelectric materials exhibit spontaneous electric polarization along a single crystallographic axis, with their ferroelectric properties and polarization switching confined to that direction.

dehydration and the complex structure of the Rochelle salt restricted the early work on ferroelectrics [32]. In 1935, the discovery of ferroelectricity in potassium dihydrogen phosphate (KH_2PO_4), abbreviated as KDP, marked a significant advancement in the field of ferroelectric materials. Contrary to Rochelle salt, KDP demonstrated the ability to maintain ferroelectric properties over a wide temperature range [32]. Nonetheless, similar to Rochelle salt, the initial applications of KDP were constrained due to both, material being fragile and water-soluble.

The discovery of ferroelectricity in Barium Titanate ($BaTiO_3$, BTO) in the mid-20th century [33] marked the beginning of the "perovskite[2] era", which witnessed intensive research into perovskite materials. BTO became a model system for studying ferroelectric behaviour due to its robust properties including its ease of synthesis, water insolubility, chemical stability at room temperature, and superior electrical properties. Table 1.1 lists the properties of various oxide materials with perovskite or layered perovskite structures that exhibit ferroelectricity. The discovery of ferroelectricity in Lead Zirconate Titanate ($Pb(Zr,Ti)O_3$, PZT) [34, 35] led to the development of ferroelectric random access memory (FeRAM) [36, 37] due to its superior ferroelectric properties that are largely independent of the crystalline quality of the material. FeRAM devices utilize the reversible polarization of ferroelectrics for data storage. In PZT, the electrical properties can be tuned for specific usage by adjusting the ratio of Zr and Ti atoms along with the donor and acceptor doping [38, 39]. The ferroelectric nature of PZT comes from the displacement of Zr or Ti elements within the perovskite structure. Despite its success, the high dielectric constant of ~ 1300, coupled with a low coercive field and challenges in integrating it into CMOS process flows, complicates the scaling down of PZT-based ferroelectric devices below 90 nm thickness [40–42].

[2] Perovskite is a crystal structure with the formula ABX_3, where A is a large cation (such as an alkali, alkaline earth, or rare earth metal), B is a smaller cation (often a transition metal), and X is typically oxygen.

Table 1.1: A list of ferroelectric materials with perovskite or layered perovskite structures and their properties. Table adapted from [43].

Compound	**Chemical formula**	**Year discovered**	**Curie temperature T_C (K)**	**Remnant polarization, P_R (μC/cm^2)**	**Crystal structure**
Barium titanate	$BaTiO_3$	1945	398	25	Tetragonal
Potassium niobate	$KNbO_3$	1949	400	20-40	Orthorhombic
Lead zirconate titanate	$PbZr_{1-x}Ti_xO_3$	1949	Depends on the composition	20-97	Tetragonal for Ti-rich, Rhombohedral for Zr-rich
Lead titanate	$PbTiO_3$	1950	763	20-96.5	Tetragonal
Lead zirconate	$PbZrO_3$	1951	503	20-50	Orthorhombic
Lead bismuth niobate	$PbBi_2Nb_2O_9$	1959	833	~3	Pseudo tetragonal
Strontium bismuth tantalite	$SrBi_2Ta_2O_9$	1960	600	30-70	Orthorhombic
Barium strontium titanate	$Ba_{0.73}Sr_{0.27}TiO_3$	1960	298	10-30	Tetragonal
Bismuth titanate	$Bi_4Ti_3O_{12}$	1961	953	10-30	Orthorhombic

The discovery of ferroelectricity in polyvinylidene fluoride (PVDF) in the 1980s introduced a new class of ferroelectric materials known as ferroelectric polymers [44, 45]. These materials combined flexibility with ferroelectric properties enabled applications in flexible electronics and enhanced the understanding of ferroelectric phenomena in such materials. These materials have been studied for their application in FeRAMs. Even though the flexible structure helps to overcome temperature instabilities, the long access time remains a disadvantage of this technology [46].

The 21st century has seen continued advancements with the emergence of multiferroics and two-dimensional ferroelectrics [47, 48]. In 2003, the discovery of room-temperature multiferroicity in epitaxial bismuth ferrite ($BiFeO_3$) thin films offered new ways to couple magnetic and electric properties, which proved to be crucial for next-generation computing and memory devices [49].

The discovery of ferroelectricity in Hafnia-based materials in 2011 [22] has attracted more attention to this field due to its ability to retain ferroelectricity even at ultra-thin dimensions allowing to overcome the scalability and CMOS-compatibility issues faced by the conventional perovskite-based ferroelectrics. Ferroelectric properties of Hafnia-based materials will be discussed in detail in the next section. Recently, the discovery of ferroelectricity in AlScN films [50] showed a high remnant polarization of 80-120 μC/cm^2 [51]. However, this material has a much higher coercive field compared to Hafnia-based ferroelectrics, requiring higher voltages for polarization switching. Considering the mature deposition techniques and the CMOS compatibility of AlScN-based material, it shows great potential towards microelectronic applications. However this discovery is fairly recent and further study is required to reduce the leakage current and the coercive field of this material for practical applications.

1.1.3 Hafnium-oxide based ferroelectric thin films

The integration of non-ferroelectric HfO_2 into CMOS processes was driven by its excellent properties as a high-k dielectric material, which helped to further miniaturize field effect transistor devices [52–54]. The discovery of ferroelectric properties in Si-doped HfO_2 thin films introduced new possibilities for ferroelectric memory devices [22], as this material facilitated the scaling down and lowered the power requirement of ferroelec-

tric devices - a challenge previously faced with traditional perovskite-based ferroelectric devices [55]. These advantages led to extensive research on this material in an attempt to enhance its properties to support the commercialization of ferroelectric memory devices.

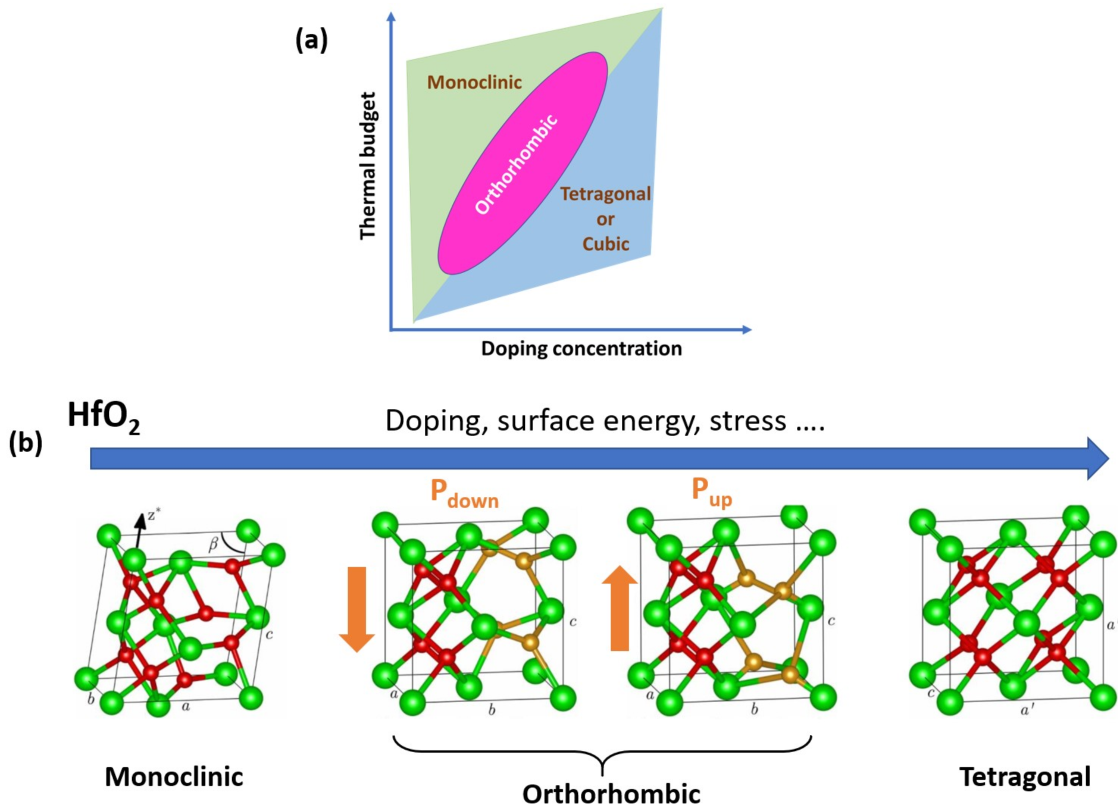

Figure 1.4: (a) Phase diagram of doped HfO_2, adapted from [9]. (b) Schematic of the mechanisms and corresponding crystal phases (m-phase, o-phase and t-phase) stabilized in the HfO_2 thin films. In this representation, Hf atoms are depicted in green, oxygen atoms in red, and oxygen atoms that determine the polarization state are shown in golden colour. Depending on the position of the golden colour oxygen atoms, two polarization states P_{down} and P_{up} are obtained in the ferroelectric o-phase. In HZO films, Zr atoms occupy some cation sites instead of Hf atoms. This mixed occupancy stabilizes the orthorhombic phase, especially with specific doping levels and annealing processes. This figure is adapted from [32, 56].

For hafnium oxide, achieving the ferroelectric phase necessitates thin films due to the structural constraints and stabilization mechanisms that occur at reduced dimensions. Ferroelectricity has been reported in HfO_2 thin films doped with many different elements such as Si, Zr, Y, Al, Gd, Sr, La, Ge and Sc [57–63]. Research also indicates that undoped HfO_2 thin films exhibit ferroelectric properties when oxygen vacancies are present in the film [56, 64]. The HfO_2 material is normally present in the stable monoclinic phase (m-phase). At high temperatures and pressure, the tetragonal (t-phase) and cubic (c-phase)

phases are stabilized in the material [55]. Neither of these phases gives rise to ferroelectricity. The ferroelectric behaviour in HfO_2 films originates from the noncentrosymmetric orthorhombic phase (o-phase, space group $Pca2_1$) [55]. This phase is not found in the equilibrium phase diagram of HfO_2. It is possible to stabilize this polar phase by tuning the amount of oxygen vacancies [65], controlled doping of different elements [57], rapid quenching [66] and mechanical stress [55]. However, it is difficult to study the impact of each of these factors independently as these factors usually coexist.

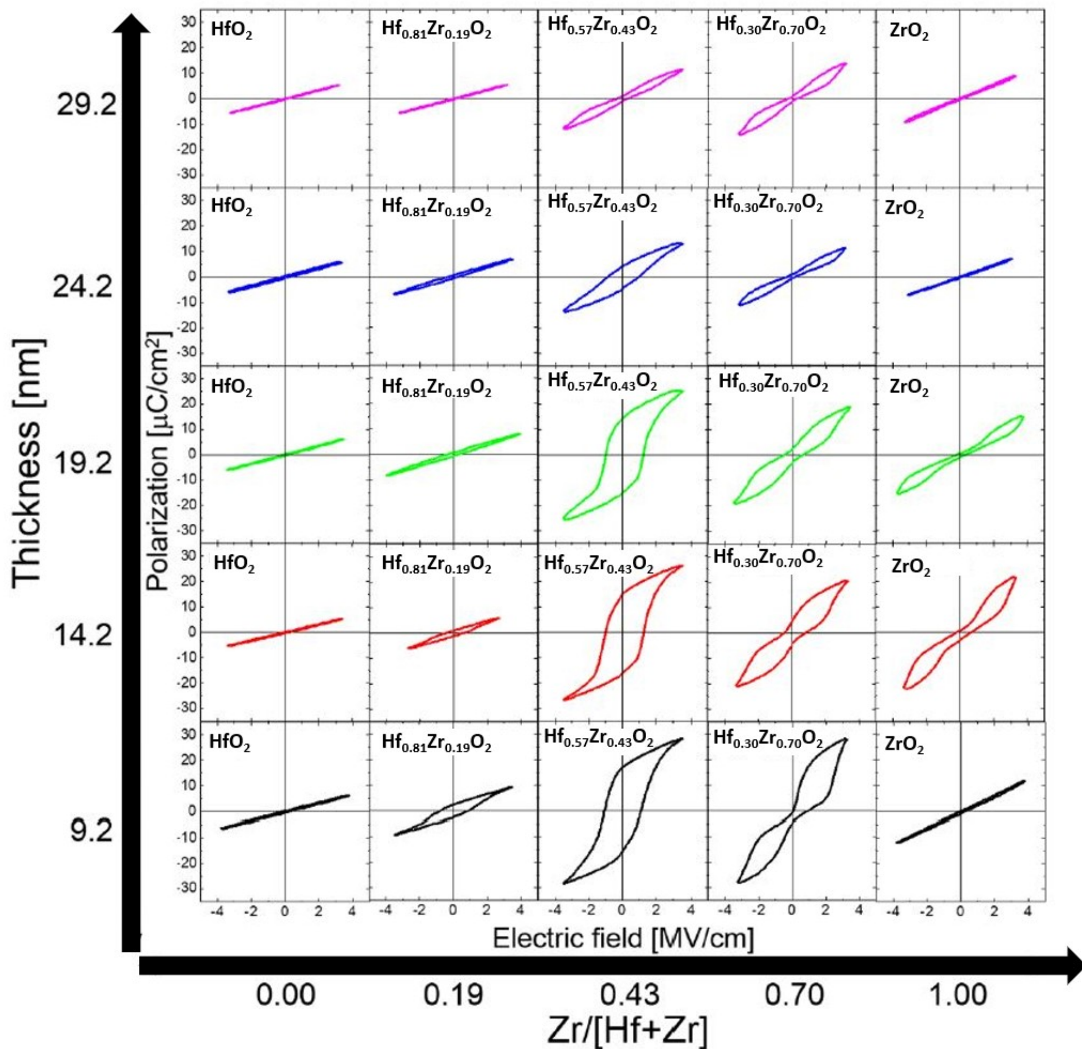

Figure 1.5: Polarization-electric field (P-E) curves for $Hf_{1-x}Zr_xO_2$ films with varying compositions and thicknesses. The top and bottom electrodes were made of Pt/TiN (with the TiN layer in contact with the dielectric) and TiN, respectively. All the tested capacitor samples were annealed at 500 °C in a nitrogen atmosphere for 30 seconds following the top electrode deposition. Figure adapted from [67].

When the oxygen supply during the deposition (physical vapour deposition (PVD) or atomic layer deposition (ALD) deposition) of HfO_2 film (10 nm) is reduced, it leads to the

generation of oxygen vacancies stabilizing the o-phase. Further increase in the amount of oxygen vacancies leads to the stabilization of the t-phase [65]. The phase diagram corresponding to the solid solution of HfO_2 film is shown in Figure 1.4(a). The dopant concentration required to stabilize the o-phase depends on dopants. Generally, the gradual increase in the dopant concentration leads to a decrease in m-phase and stabilizes the o-phase. Further increase in the dopant concentration leads to the stabilization of t-phase or c-phase [41]. In the ferroelectric o-phase of HfO_2, the oxygen atoms can occupy two stable positions, shifting up or down in response to the polarity of an externally applied electric field. Depending on the orientation of these oxygen atoms, a permanent electric dipole is established that can point either upwards (P_{up}) or downwards (P_{down}) as shown in Figure 1.4(b).

Among the different dopants used for attaining stable o-phase in the Hafnia-based thin film, Zr is the most promising [55]. $Hf_{1-x}Zr_xO_2$ thin films show ferroelectric properties for a wide range of doping concentrations, making the process very flexible [67]. Hf and Zr share very similar physical and chemical properties. As a result, the optimal doping concentration of Zr to achieve the highest remnant polarization is around 50% (shown in Figure 1.5 for different film thicknesses), while for other dopants (e.g., La), a significantly lower concentration is required to attain similar effects [23, 61, 68]. Hence, obtaining homogenous and reproducible ferroelectric thin films with Hf:Zr ratio of 1:1 is relatively easy compared to other ratios required for different dopants using atomic layer deposition (ALD) technique. This is due to the vertical inhomogenous doping effect in ALD [55]. From Figure 1.5, it is clear that $Hf_{1-x}Zr_xO_2$ films show ferroelectric properties when x$\sim$0.5 due to the stabilization of o-phase even at a smaller thickness of 9.2 nm. As the Zr compositional ratio (x) increases from 0 to 1, the film starts to show nonlinear dielectric properties for film thicknesses of 9.2 nm to 29.2 nm. When the x value is in the range of 0.3 to 0.5, the film shows ferroelectric behaviour and when it is in the range of 0.7 to 1, the film shows antiferroelectric-like behaviour [55]. Hf-rich films crystallize in the m-phase, whereas Zr-rich films crystallize in the t-phase. This trend has been reported in many studies [55, 69]. The $Hf_{0.5}Zr_{0.5}O_2$ (HZO) thin films can be crystallized in ferroelectric o-phase at a relatively lower processing temperature ($\sim$ 400 °C) [70], whereas the other dopants require much higher heat treatment ($>$ 650 °C) for stabilizing

the o-phase [55, 68]. This characteristic allows ferroelectric HZO to be compatible with the CMOS back-end-of-line.

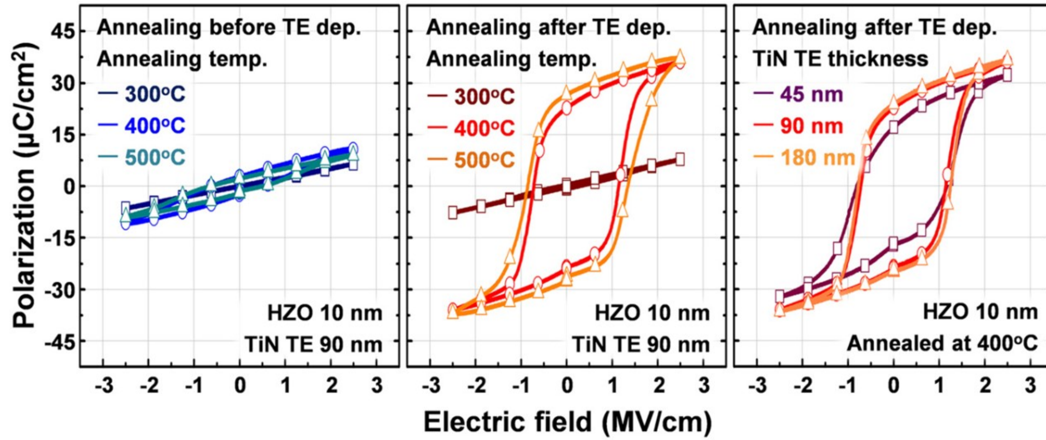

Figure 1.6: P-E hysteresis curve from TiN-HZO(10 nm)-TiN stack after wake-up of 10^5 cycles (wake-up cycling with 2.5 MV/cm) annealed at 300 °C to 500 °C before and after TiN top electrode deposition. Figure reproduced from [71].

The HZO films crystallize between the bottom and top electrodes, which apply mechanical stress to the HZO film, influencing the stabilization of the ferroelectric o-phase. As shown in Figure 1.6, 10 nm HZO film crystallized with the presence of TiN top electrode showed higher remnant polarization compared to the HZO film crystallized in the absence of TiN top electrode at different annealing temperatures ranging from 300 °C to 500 °C. This was because the crystallization of HZO in the absence of TiN top electrode was leading to the formation of o-phase along with m-phase in the film. Whereas when the film was crystallized with the TiN top electrode, o-phase with crystallographic orientation along (111) plane was obtained [71]. The thickness of the TiN top electrode also influenced the ferroelectric nature of the HZO thin film. An increase in TiN top electrode thickness also increases the o-phase ratio in HZO [55]. Researchers have extensively studied the role of different electrodes and their thicknesses on the ferroelectric properties of HZO films by providing the mechanical stress needed to stabilize the o-phase [72–75]. The mechanical stress is imparted to the film through the engineering of the capping layer or by adjusting the thermal expansion coefficient of the substrate based on the choice of electrodes, which affect the orientation and grain size of the HZO films [71, 76–82]. It is well established that the use of TiN top electrode (a favoured material for mass production) provides tensile stress to the HZO film during annealing, which helps in the

stabilization of o-phase [71, 72, 79].

1.1.4 Models of polarization switching mechanisms

Polarization switching in ferroelectric materials is a complex process characterized by the formation and growth of domains within the material ([83], see Figure 1.7(a)-(e)). This process is critical for the functioning of ferroelectric devices. Polarization switching can be initiated by applying an external voltage, which reorients the dipoles in the ferroelectric material, resulting in a change in its polarization state. The dynamics of this process can be described through various theoretical models, each providing insights into different aspects of domain behaviour and switching kinetics. Understanding models of polarization switching mechanisms is crucial as it provides insights into the fundamental behaviours of ferroelectric materials used in ferroelectric memory devices.

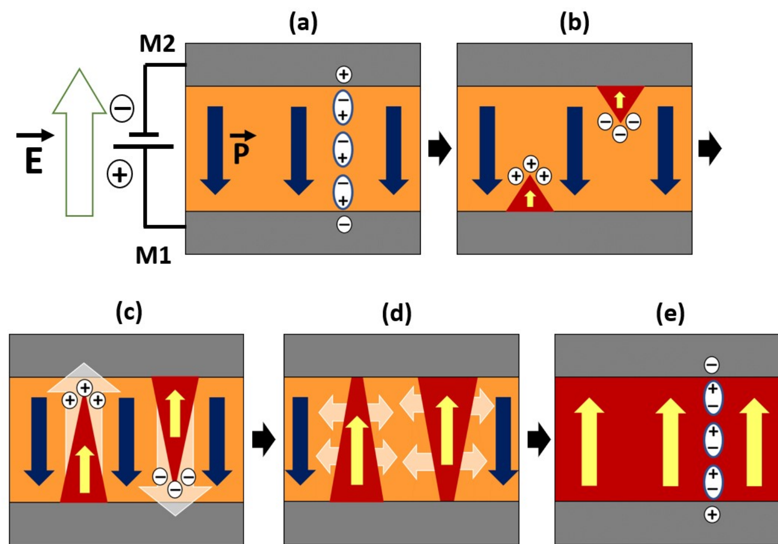

Figure 1.7: Schematic of polarization switching process under an applied electric field E [83]. (a) Initially, the polarization is fully oriented downwards. (b) Upon exceeding a certain voltage threshold, nucleation of a flipped domain begins. (c) Driven by charges at the domain wall, the flipped domain rapidly propagates. (d) As polarization aligns mostly parallel to the domain wall, a more energetically stable state is achieved, resulting in slow lateral growth. (e) The domain is fully switched.

Merz's law

Merz's law is a fundamental relation that describes the correlation between the switching time (τ) and the applied electric field (E) [84]. According to this law, the switching time

is exponentially related to the activation field (E_a) required for polarization reversal:

$$\tau = \tau_0 \cdot \exp\left(\frac{E_a}{E}\right) \tag{1.4}$$

where τ_0 is the intrinsic switching time. Notably, E_a is temperature-dependent. This relationship indicates that films with a higher activation field will require a longer time to switch their polarization state for a given applied field. However, Merz's law does not provide a detailed mechanism for the switching process, prompting the development of more sophisticated models.

Kolmogorov-Avrami-Ishibashi (KAI) model

In this model, domain nucleation occurs instantaneously throughout the material [85]. Once nucleated, domain walls move horizontally, causing the domain to expand until it encounters another domain wall [86]. The time-dependent polarization change (Δ P(t)) in this model is given by:

$$\Delta P(t) = 2P_s[1 - \exp(-\left(\frac{t}{\tau}\right)^n], \tag{1.5}$$

where P_s is the spontaneous polarization and n is an effective dimensionality factor. Here, τ is the total switching time. This model suggests that domain expansion is the most time consuming aspect of polarization switching. KAI model is commonly applied to describe the behaviour of traditional single-crystal perovskite ferroelectrics [87, 88] and epitaxial thin film ferroelectrics [89]. However, this model fails to accurately describe the domain reversal behaviour in polycrystalline ferroelectric thin films, particularly at low applied fields [90–92].

Nucleation-limited switching (NLS) model

In thin HfO_2-based ferroelectric films, which typically exhibit a polycrystalline structure, the nucleation-limited switching (NLS) model provides a more accurate description. Due to the presence of multiple grains and potential defects, domain propagation is limited, leading to numerous nucleation events with small nuclei sizes [92–94]. These nucleation sites can include grain boundaries, interfaces, and impurities. The NLS model suggests

that many nucleation events occur simultaneously, and the growth rate of these nuclei depends on both volume and surface energy contributions. The switching field is assumed to be proportional to the coercive field (E_C), and the relationship between the coercive field and the ferroelectric layer thickness (d_{FE}) is given by [95]:

$$E_C \propto d_{FE}^{-2/3} \tag{1.6}$$

This relationship holds until a saturation plateau is reached, beyond which E_C becomes independent of layer thickness and is instead determined by grain size. The KAI model treats the switching time τ as a constant fitting parameter, while the NLS model proposes that the switching time follows a Lorentzian distribution. For the NLS model, the time-dependent polarization switching is formulated as [96],

$$\Delta P(t) = 2P_s \int [1 - \exp(-\left(\frac{t}{\tau}\right)^n] \, F(\log\tau) \, d(\log\tau), \tag{1.7}$$

where

$$F(\log\tau) = \frac{A}{\pi}\left(\frac{\omega}{(\log\tau - \log\tau_1)^2 + \omega^2}\right). \tag{1.8}$$

Here A is the normalized constant, ω is the half-width at half-maximum of the distribution and $\log(\tau_1)$ is the median logarithmic value of the distribution. According to this model, nucleation events dominate the polarization switching kinetics. This model is extensively used in the literature to describe polarization reversal in both traditional perovskites and HfO_2-based films [93, 97–99].

Landau-Devonshire theory

From a thermodynamic perspective, the Landau-Devonshire theory provides a macroscopic description of polarization switching [100]. It considers the free energy landscape of a ferroelectric material, where two energy minima correspond to the two stable polarization states. An external electric field is required to overcome the energy barrier between these states. This theory assumes that the coercive field is intrinsic and independent of the switching duration, which contrasts with experimental observations showing a time-voltage correlation [41]. To reconcile these discrepancies, the multi-grain Landau-Khalatnikov approach was developed for HfO_2-based ferroelectrics [101]. This approach

incorporates a time-dependence by considering a distribution of local fields averaged over multiple regions within the ferroelectric film. This model accounts for the macroscopic behaviour of polarization switching in polycrystalline materials.

1.1.5 Ferroelectricity for memory applications

In ferroelectric materials, the spontaneous polarization can be reversed by applying an external electric field. When an electric field of sufficient magnitude is applied in the direction opposite to the initial polarization, the domains within the ferroelectric material realign to switch the polarization direction. This switching mechanism is highly stable and non-volatile, meaning the polarization state remains even after the electric field is removed. As shown in Figure 1.8, this bistability forms the basis of binary memory devices, where the two polarization states are used to encode binary information.

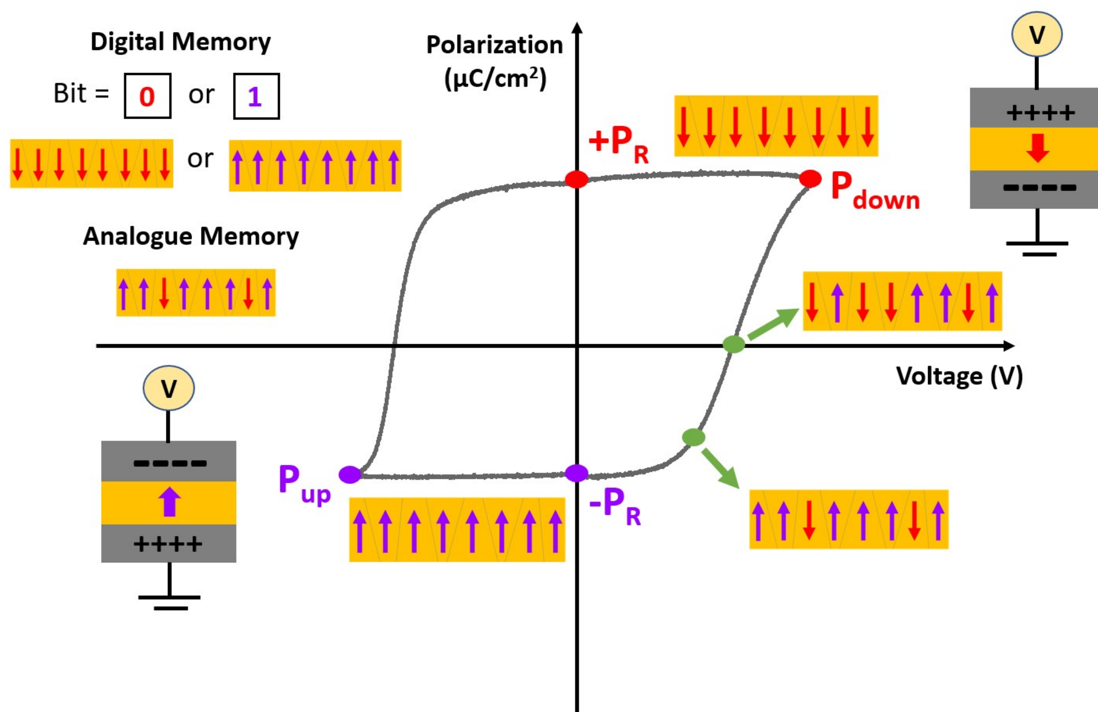

Figure 1.8: Schematic representation of utilizing ferroelectric properties for binary and analog memory applications. Aligning all dipoles in the down or up direction facilitates binary data storage as '0' or '1' bits. In contrast, applying a lower magnitude electric field achieves partial domain switching, enabling analog memory applications.

The ferroelectric domain switching is not always an all-or-nothing process. When a lower magnitude electric field is applied, it can cause partial switching of domains, leading to intermediate polarization states. This partial or gradual switching is a result of

the complex interplay between different domains within the ferroelectric material. By precisely controlling the applied electric field, it is possible to achieve a range of stable polarization states between the fully polarized P_{up} and P_{down} states. Ferroelectric memory devices utilize this gradual switching capability to store data in a continuous manner. Instead of representing data as a simple 0 or 1 (binary form), these memories can store a range of values, leading to multiple resistance states. This is particularly useful in applications such as neuromorphic computing and in high-resolution data storage solutions. There are three types of ferroelectric memory devices that utilize ferroelectric materials for data storage. While they share similarities in their programming principles, they differ in their structures and working mechanisms.

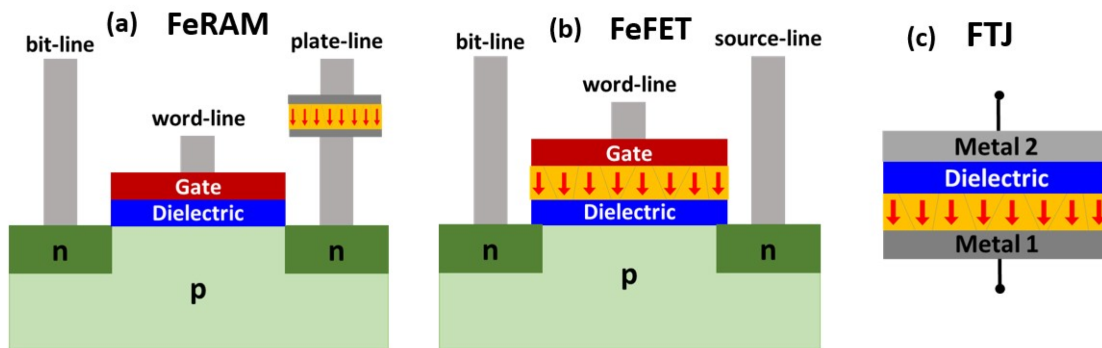

Figure 1.9: Schematic representation of (a)1T–1C FeRAM device, (b) FeFET device and (c) FTJ device.

- **Ferroelectric random access memory (FeRAM)**: In FeRAM, each memory cell consists of a ferroelectric capacitor paired with a transistor as shown in Figure 1.9(a). This type of architecture is called 1T-1C memory cell. In FeRAMs, the data is stored in the ferroelectric capacitor and the transistor connected to it acts as a switch. The two different polarization states of the ferroelectric materials can be used within a capacitor to create two states for a memory cell. The read operation of FeRAM involves a sequence of stages, closely resembling the process used in DRAM. Initially, the memory cell is in an inactive state with the bit line, plate line, and word line all set to low. To initiate the read operation, voltages are applied to the word line and plate line. This places an electric field across the ferroelectric capacitor, causing it to either switch or remain in its current state, depending on the stored data. If the capacitor switches, it induces a charge that is shared with

the bit line capacitance. The resulting bit line voltage is proportional to the ratio of the switched capacitance (C_s) to the bit line capacitance (C_{bit}). This voltage is then compared to a reference voltage using a sense amplifier, which amplifies the difference to determine whether the stored bit is a logic '0' or '1'. Since reading the cell can alter its state, FeRAM employs a process to restore the original data immediately after the read operation, ensuring data integrity.

The write operation in FeRAM also leverages the unique properties of ferroelectric materials. To write data, the control circuitry applies a field across the ferroelectric capacitor in the desired direction, switching its polarization state to represent either a binary '0' or '1'. This data remains intact even when power is removed due to the non-volatile nature of ferroelectric materials. Unlike DRAM, where the charge gradually leaks away, the polarization state in FeRAM does not degrade over time, providing indefinite data retention. The first demonstration of non-volatile DRAM (FeRAM) was done recently [102]. It has just begun to be shown in high densities as a commercial DRAM technology.

- **Ferroelectric field effect transistor (FeFET)**: The FeFET consists of a 1T memory cell. Its structure includes a source and bit line, a gate electrode, and a ferroelectric layer sandwiched between the gate electrode and the channel, as shown in Figure 1.9(b). This ferroelectric layer exhibits stable polarization states that can be reversed by an external electric field.

  The writing process in FeFETs involves setting the polarization state of the ferroelectric layer to store data. This is done by applying a voltage to the gate while grounding the bulk, with the source and drain either floating or at a fixed potential. This ensures effective polarization switching without interference from current flow through the source and drain. If the desired data bit is a logic '1', a positive voltage is applied to the gate, causing the electric field to align the dipoles in the ferroelectric material in one direction. Conversely, if the desired data bit is a logic '0', a negative voltage is applied, aligning the dipoles in the opposite direction. This alignment of dipoles creates a corresponding electric field within the ferroelectric layer, which modulates the threshold voltage of the transistor. The polarization state remains stable even after the removal of the applied voltage due to the non-volatile

nature of the ferroelectric material. This ensures that the data is retained without the need for a continuous power supply.

The read operation in FeFETs involves identifying the current through the transistor and associating it with a state of polarization to retrieve the stored data. During a read operation, a small voltage is applied between the source and drain terminals of the transistor and the gate voltage is set to a level that allows the transistor to either conduct or remain non-conductive based on the polarization state. If the ferroelectric layer's polarization corresponds to a logic '1', the transistor's threshold voltage is altered in a way that allows current to flow through the channel. If the polarization corresponds to a logic '0', the threshold voltage remains high, preventing current flow.

The critical aspect of the FeFET read mechanism is that it is non-destructive, that is, the polarization state of the ferroelectric material is not altered during the read process. This ensures that the data remains intact and can be read multiple times without degradation. The FeFET concept faces notable retention challenges due to charge trapping and depolarization field effects at the dielectric interface between the ferroelectric layer and the semiconductor channel. These retention issues compromise the reliability of FeFETs and must be resolved to facilitate the successful commercial integration of 1T cells. However, recent advancements have shown that FeFETs can achieve multiple resistance states through cumulative switching [103]. This breakthrough opens up new possibilities for FeFETs in neuromorphic computing and logic-in-memory applications, significantly increasing interest in these devices.

- **Ferroelectric tunnel junction (FTJ)**: FTJs utilize the unique properties of ferroelectric materials and quantum tunneling to store data. An FTJ device consists of a ferroelectric layer or a combination of ferroelectric and dielectric layers sandwiched between two metallic electrodes, creating a capacitor-like structure as shown in 1.9(c). The polarization of the ferroelectric layer controls the FTJ device's tunneling current. High resistance at a specific read voltage indicates logic '0', and low resistance indicates logic '1'. Data writing is accomplished by switching the polarization of the ferroelectric layer to either the up or down direction, while reading is

performed by measuring the current flowing through the stack at a voltage smaller than the positive or negative coercive voltage.

FTJs offer several advantages over other ferroelectric memory technologies such as FeRAM and FeFETs. Compared to FeRAM, FTJs are superior due to their non-destructive readout mechanism and enhanced scalability, enabling higher memory density and a reduced physical footprint. FTJs outperform FeFETs with their simpler two-terminal structure, which reduces fabrication complexity. Additionally, FTJs exhibit lower power consumption, better retention, and superior endurance properties. They also feature fast switching speeds, making them suitable for high-speed, energy-efficient applications. FTJs can achieve multilevel cell capability by storing multiple bits per cell through intermediate resistance states, further enhancing storage density. Their straightforward fabrication process is compatible with existing semiconductor manufacturing techniques, facilitating easier integration into current technology nodes. This thesis focuses on FTJ memory devices and their working mechanisms which will be discussed in detail in the following section.

1.2 Ferroelectric tunnel junction (FTJ)

A typical FTJ consists of two metal layers separated by a thin ferroelectric insulating barrier, see Figure 1.9(c). Although classically forbidden, electrons can traverse this potential barrier if its height exceeds the electron's energy through quantum mechanical tunnelling. The profile of the ferroelectric potential barrier depends on the direction of polarization in the ferroelectric layer, resulting in different tunnel resistances for the two polarization directions. However, the tunnelling probability becomes significant only when the barrier is ultrathin, typically just a few nanometers thick. The concept of FTJs was first introduced by Esaki et al. in 1971 [104], who predicted a change in tunnel resistance upon ferroelectric polarization switching. Achieving this goal presents significant challenges, primarily because it necessitates the creation of ultrathin films that retain strong ferroelectric properties at thicknesses of only a few unit cells. It was not until the early 2000s that substantial progress was made. In 2005, Kohlstedt et al. [105] and Zhuravlev et al. [106]

conducted theoretical investigations into the current-voltage characteristics of FTJs, providing a crucial understanding of their behaviour. Following this, in 2006, Tsymbal and Kohlstedt proposed mechanisms contributing to resistance changes, enhancing the theoretical framework for FTJs [107].

The first experimental demonstration of FTJs using multiferroic barriers was achieved by Gajek et al. in 2007 with $La_{0.1}Bi_{0.9}MnO_3$ (LBMO) films [108]. This was followed by significant experimental advancements in 2009 and 2010, when Gruverman and Crassous demonstrated FTJs using $BaTiO_3$ [109] and $PbTiO_3$ [110], respectively. In 2009, Garcia demonstrated the non-destructive readout of ferroelectric states on an FTJ device based on a highly strained $BaTiO_3$ ultrathin film (3nm thick), which is a critical feature for practical memory devices [111].

A pivotal moment came in 2014 when Li et al. reported the first epitaxial FTJ on silicon [112]. This breakthrough demonstrated the potential for integrating FTJs with existing silicon technology, a crucial step for their application in conventional semiconductor processes. In 2015, Guo further demonstrated functional FTJ devices on silicon with good performance, underscoring the practical viability of FTJ technology [113]. However, integrating FTJs with ultrathin perovskite ferroelectric films into conventional silicon-based memory technology faces several challenges, such as poor interfacing with silicon, high crystallization temperatures, and electrical degradation from forming gas treatments [114]. HfO_2-based ferroelectric materials offer a solution to these issues. In 2017, Ambriz-Vargas et al. successfully fabricated an FTJ using a CMOS-compatible $Hf_{0.5}Zr_{0.5}O_2$ tunnel barrier on a TiN electrode, demonstrating its potential for seamless integration into silicon-based memory technologies [115]. In the same year, research by Boyn et.al on solid-state synaptic learning based on FTJs with $BiFeO_3$ as a ferroelectric layer, demonstrated its potential for neuromorphic computing applications, where they could mimic synaptic activities of the human brain [116]. This was further advanced in 2018 by Guo et.al, who demonstrated synaptic learning in FTJs based on $BaTiO_3$, solidifying its role in advanced computational architectures [117]. This work also demonstrated that interface plays a vital role in the functioning of FTJs. Through interface engineering once can adjust the intrinsic band alignment of the ferroelectric/metal-semiconductor heterostructure, resulting in varied resistive switching processes. In 2019, Kobayashi et al.

demonstrated multi-level operation on FTJ devices using a 4 nm thick ferroelectric HZO layer [118].

As previously mentioned, achieving high remnant polarization at a small thickness (1-4 nm), a requirement for high performing FTJ device, is challenging and as an alternative, a new device architecture was demonstrated by Max et.al in 2019 with HZO ferroelectric layer and Al_2O_3 dielectric layer [119]. Instead of using a metal-ferroelectric-metal (M-FE-M) stack, it used a metal-ferroelectric-dielectric-metal (M-FE-DE-M) architecture. The novelty of this type of stack was first proposed and proven by Meyer et.al in 2004 as a ferroresistive RAM [120]. In this case, the HZO ferroelectric layer serves as the memory layer, where the information is stored as the polarization state and the dielectric layer serves as the tunnelling barrier for electron conduction. This study highlighted the direct correlation between memory properties and phenomena such as wake-up and fatigue in the ferroelectric layer and suggested that optimizing the ferroelectric/dielectric interface could improve the viability of FTJs for memory applications. In the same year, Ryu et al. demonstrated that FTJ devices based on an HZO ferroelectric layer with an M-FE-DE-M architecture could be used for neuromorphic applications [121]. They achieved multiple resistance states through pulse modification, showcasing the potential of these devices for advanced computing applications.

Despite these advancements, there are still challenges to be addressed for the commercial viability of Hafnia-based FTJ devices. Key issues include improving the reliability and endurance of the devices, ensuring uniformity in large-scale production, and further integrating FTJs with existing semiconductor technologies. Continued research and development are expected to overcome these challenges, paving the way for FTJs to become a standard component in high-density memory storage and neuromorphic computing applications. This thesis work began in January 2020, aiming to develop FTJ devices with an HZO ferroelectric layer and integrate them into the CMOS back end of line with application to neuromorphic computing.

1.2.1 Physics of FTJ devices

In its very simple form, an FTJ device consists of a ferroelectric layer located between two dissimilar metal electrodes as shown in Figure 1.10(a). The two polarization directions of

the ferroelectric layer leads to two different resistance states as shown in Figure 1.10(b). This phenomenon is known as the tunnelling electroresistance (TER) effect [122]. The screening length refers to the distance within a metal over which mobile charge carriers (electrons) can neutralize the electric field caused by an external charge. It is a measure of how effectively a metal can screen or mitigate the electric fields emanating from the ferroelectric layer. The two metal electrodes (Metal 1 and Metal 2) have a different screening lengths (δ_1 and δ_2). The polarization charges are screened by the screening charges per unit area (σ_s), shown in Figure 1.10(c). According to Thomas-Fermi model, this can de defined as,

$$\sigma_{\mathrm{s}} = \frac{\mathrm{Pd}}{\epsilon_{\mathrm{b}}\left(\frac{\delta_1}{\epsilon_1} + \frac{\delta_2}{\epsilon_2}\right) + \mathrm{d}}, \tag{1.9}$$

where P is the ferroelectric polarization, d is the ferroelectric thickness, ϵ_1, ϵ_2 and ϵ_b are the static dielectric constants of Metal 1, Metal 2 and barrier, respectively [123].

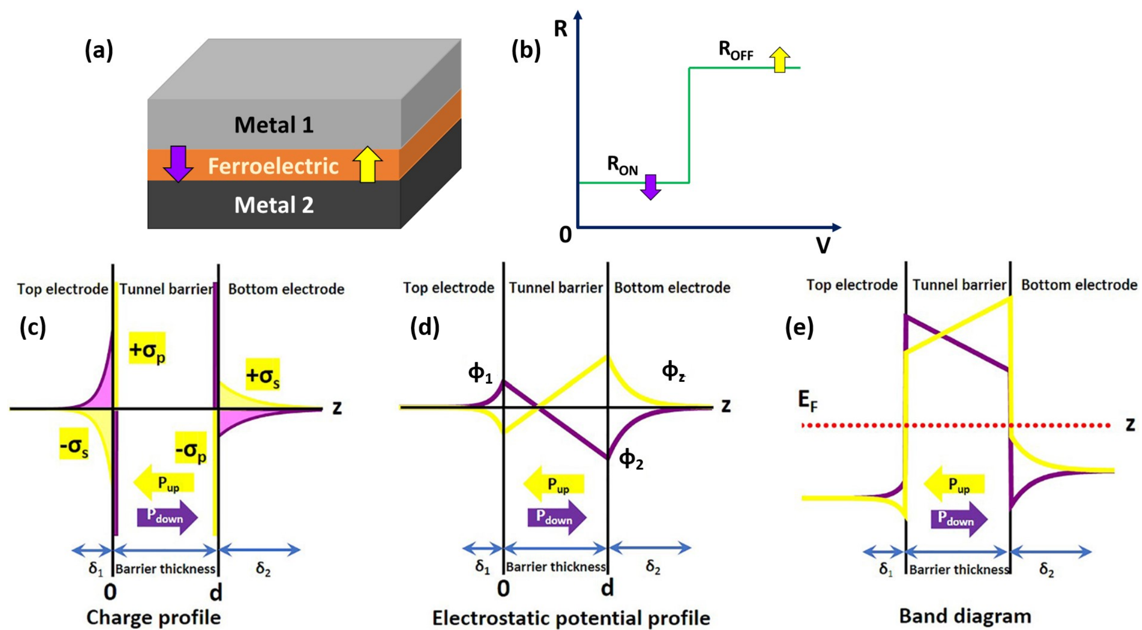

Figure 1.10: Schematic of (a) the FTJ structure and (b) the two resistance states $\mathrm{R}_{\mathrm{OFF}}$ and R_{ON} of FTJs through polarization switching. (c) Charge distribution, (d) the corresponding electrostatic potential profile, and (e) the band diagram of an M1-FE-M2 FTJ with different polarization directions. It is assumed that the screening length of metal 1 is shorter than that of metal 2, resulting in an asymmetry in the potential profile. Yellow and purple colours indicate different polarization directions. Figure adapted from [123].

Due to the incomplete screening of the bound charges, an electrostatic potential ($\phi(\mathrm{z})$) arises within the M-FE-M stack as shown in Figure 1.10(d) and it can be defined as,

$$\phi(z) = \begin{cases} \frac{\sigma_s \delta_1}{\epsilon_0} e^{-\left(\frac{|z|}{\delta_1}\right)}, & z \leq 0 \\ \\ -\frac{\sigma_s \delta_2}{\epsilon_0} e^{-\left(\frac{z-d}{\delta_2}\right)}, & z \geq d \end{cases}. \tag{1.10}$$

When the electrostatic potential is incorporated into the M1-FE-M2 equilibrium band diagram, it results in a band profile illustrated in Figure 1.10(e). The energy barrier profile $\mathrm{E_b}(\mathrm{z})$ is determined by the interfacial barrier heights that are composed of the initial barriers $\varphi_{\mathrm{B},1}$ at the M1 interface, $\varphi_{\mathrm{B},2}$ at the M2 interface and the changes induced by the screening charges $-e\phi_{1,2}$ in the metallic electrodes depending on the polarization. The barriers at the interface of the metal $\mathrm{i} \in \{1, 2\}$ are defined by the difference of metal work function ($\mathrm{WF_i}$) and the electron affinity (χ) of the ferroelectric [28].

$$\varphi_{\mathrm{B,i}} = \mathrm{WF_i} - \chi. \tag{1.11}$$

Due to the different screening lengths of the top and bottom electrodes, the potential profile for opposite polarization directions is asymmetric. As a result, the potential experienced by transport electrons changes with the switching of ferroelectric polarization, leading to the TER effect, which can be expressed as follows:

$$\mathrm{TER} = \frac{\mathrm{I_{ON}} - \mathrm{I_{OFF}}}{\mathrm{I_{OFF}}}. \tag{1.12}$$

Even though this model explains the TER effect based on the screening effect, theoretical and experimental studies indicate that interface effects, strain effects, and oxygen vacancy migration contribute to resistive switching in FTJs [105, 107]. Polarization reversal, inverse piezoelectric effects, and oxygen vacancy movement affect ion positions, film thickness, tunnelling barrier width, and transmission probability [123, 124]. Additionally, electrode and interface properties also impact resistive switching in FTJs [125–127]. The incomplete screening of polarization charges can generate an electric field opposing the polarization direction, known as the depolarization field. It is defined as [118],

$$\mathrm{E_{depol}} = -\frac{\mathrm{P} - \sigma_{\mathrm{s}}}{\epsilon_0\ \epsilon_{\mathrm{b}}}. \tag{1.13}$$

This field can destabilize the polarization states, affecting the FTJ's overall performance

by influencing the tunneling electroresistance effect and the retention of polarization states. Therefore, for practical applications, it is essential for the depolarization field to be much smaller than the coercive field.

1.2.2 Mechanisms of charge transport in FTJs

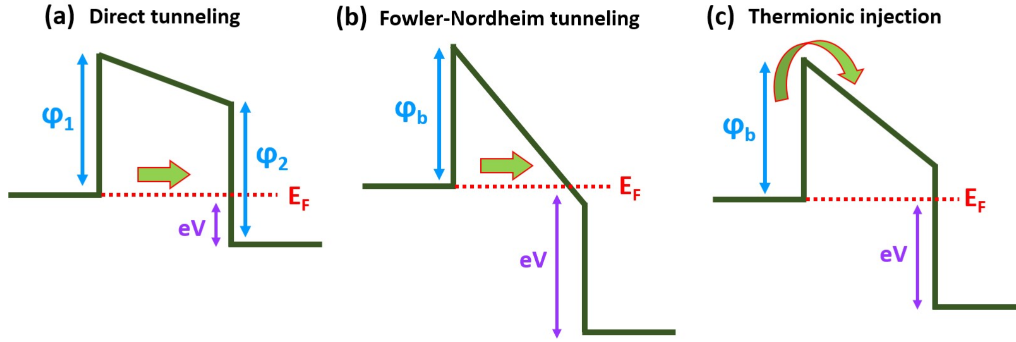

Figure 1.11: Illustrations of band diagrams depicting: (a) direct tunneling, (b) Fowler-Nordheim tunneling, and (c) thermionic injection.

Ferroelectric materials are insulating layers with a bandgap that prevents electron conduction. However, when the barrier is only a few nanometers thick, quantum-mechanical tunnelling can occur. In FTJs, direct tunnelling (DT) is a quantum process occurring in these ultra-thin films [123]. The screening of polarization surface charges alters the electrostatic potential profile, effectively changing the interfacial energy barrier. This modification results in different interfacial barrier heights at the top and bottom electrodes, denoted as φ_1 and φ_2, creating an asymmetric barrier profile as shown in Figure 1.11(a). For a trapezoidal potential barrier, the current density$\mathrm{j_{DT}}$ associated with direct tunneling at an applied voltage V, can be expressed using the Wentzel-Kramers-Brillouin (WKB) approximation as,

$$\begin{aligned}\mathrm{j_{DT}(V)} = -&\frac{4em^*_{e,b}\exp\left[\alpha(V)\left(\left(\varphi_2 - \frac{eV}{2}\right)^{3/2} - \left(\varphi_1 + \frac{eV}{2}\right)^{3/2}\right)\right]}{9\pi^2\hbar^3\left[\alpha(V)\right]^2\left[\sqrt{\varphi_2 - \frac{eV}{2}} - \sqrt{\varphi_1 + \frac{eV}{2}}\right]^2} \\ &\times \sinh\left[\frac{3eV}{4}\alpha(V)\left(\sqrt{\varphi_2 - \frac{eV}{2}} - \sqrt{\varphi_1 + \frac{eV}{2}}\right)\right].\end{aligned} \tag{1.14}$$

where,

$$\alpha(\mathrm{V}) = \frac{4\mathrm{d}\sqrt{2\mathrm{m}^*_{\mathrm{e,b}}}}{3\hbar(\varphi_1 + \mathrm{eV} - \varphi_2)}. \tag{1.15}$$

Here, $\mathrm{m}^*_{\mathrm{e,b}}$ represents the effective mass of the tunnelling electron in the barrier, e denotes the electron charge, $\hbar$ is the reduced Planck constant, φ_1 and φ_2 are the energy barrier heights on the left and right sides, d is the barrier thickness, and V is the applied voltage.

Fowler-Nordheim tunnelling (FNT) is similar to direct tunnelling but occurs at higher voltage levels [28, 123]. When the applied voltage surpasses the interfacial barrier height, a portion of the energy barrier falls below the electrode's Fermi energy level, altering the effective tunneling barrier width. As illustrated in 1.11(b), the electrons have to tunnel through a triangular-shaped potential barrier. The commonly used equation for the current density $\mathrm{j_{FNT}}$ as a function of the applied electric field (E) in the FNT regime is expressed as:

$$\mathrm{j_{FNT}}(\mathrm{E}) = \frac{\mathrm{e}^3\mathrm{E}^2}{16\pi^2\hbar\varphi_\mathrm{b}} \exp\left[-\frac{4\sqrt{2\mathrm{m}^*}\varphi_\mathrm{b}^{3/2}}{3\mathrm{e}\hbar\mathrm{E}}\right], \tag{1.16}$$

where φ_b is the potential barrier height and m^* denotes the effective mass of the tunnelling charge carrier.

Thermionic injection (TI) occurs when charge carriers overcome the potential barrier through thermal excitation at temperatures above absolute zero [28]. The barrier height is reduced by image force lowering, known as the Schottky barrier, as illustrated in 1.11(c). Here, the current density $\mathrm{j_{TI}}$ under an applied electric field (E) can be described by:

$$\mathrm{j_{TI}}(\mathrm{V}) = \mathrm{A}^{**}\mathrm{T}^2 \exp\left[-\frac{1}{\mathrm{k_B T}}\left(\varphi_\mathrm{b} - \sqrt{\frac{\mathrm{e}^3\mathrm{E}}{4\pi\epsilon_0\epsilon_\mathrm{ifl}}}\right)\right] \tag{1.17}$$

Here, A^{**} is the effective Richardson constant, φ_b is the potential barrier height, T is the temperature and ϵ_ifl is the permittivity of the ferroelectric material responsible for image force lowering.

The transport of carriers in FTJs is governed by these three mechanisms. Their contributions vary based on the ferroelectric film thickness, applied voltage, polarization direction, and material properties.

1.2.3 M-FE-DE-M device architecture for FTJs

In an M-FE-M FTJ device, electron tunnelling occurs across the ferroelectric barrier, with band alignment varying between the two polarization directions. For this configuration to function effectively, the ferroelectric layer must be less than 5 nm thick while maintaining a high remnant polarization [128]. This ensures a substantial difference between the band profiles of the high resistance and low resistance states. Recent studies have demonstrated stable ferroelectric polarization in the HfO_2-ZrO_2 solid solution system at thicknesses as low as ∼1 nm [129, 130]. However, maintaining high remnant polarization in such ultra-thin layers remains a challenge. As an alternative, a metal-ferroelectric (FE)-dielectric (DE)-metal stack can be used for FTJ devices [119, 127]. This architecture allows for a high ON/OFF ratio with a thicker FE layer, typically around 10 nm. In the M-FE-DE-M stack, charge carriers tunnel across the DE layer, which is usually 1-4 nm thick [119,121]. The tunnelling current through the dielectric is directly correlated with the polarization in the FE layer.

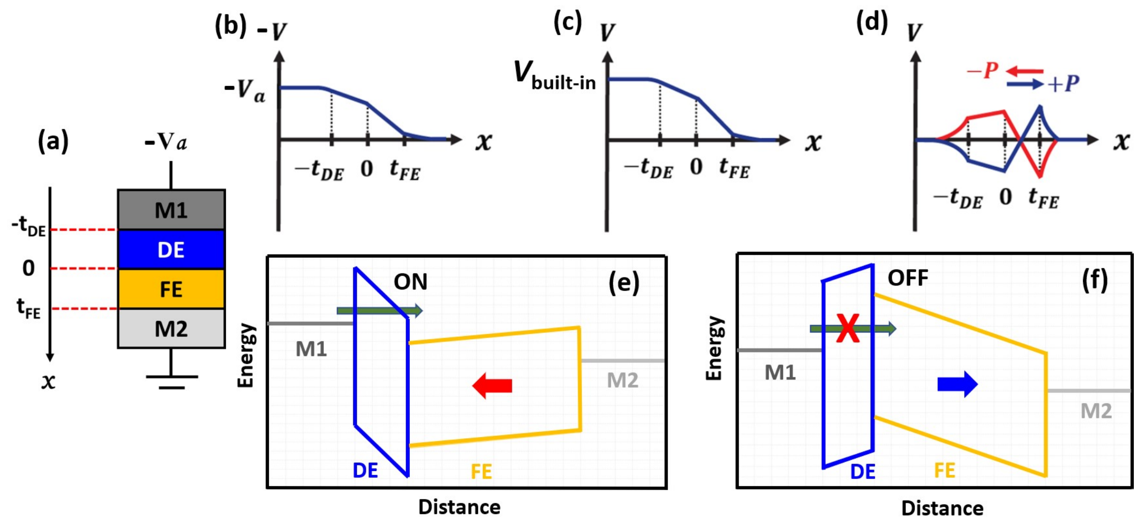

Figure 1.12: (a) Schematic of M1-DE-FE-M2 FTJ stack. Diagrams of electrostatic potential profiles resulting from (b) an applied electric field, (c) a built-in field, and (d) a depolarization field in the FTJ stack. (e) Band diagram corresponding to the low resistance state when polarization is directed towards the DE. (f) Band diagram corresponding to the high resistance state when polarization is directed away from the DE. Here, (b), (c) and (d) are adapted from [131].

A schematic of the FTJ device with M1-DE-FE-M2 architecture is shown in Figure 1.12(a). Here, M1 is the top electrode with an applied voltage of -V_a, while M2 is the bottom electrode, which is grounded. The voltage applied to the top electrode is distributed

across the dielectric and ferroelectric layers. The voltage drop across each layer depends on their respective thicknesses, dielectric constants, and the area of the FTJ device. Figure 1.12(b) qualitatively illustrates the applied voltage distribution across the stack. In this scenario, the applied voltage is less than the coercive voltage, meaning it is insufficient to cause polarization switching in the ferroelectric material. As a result, the polarization state remains unchanged despite the applied voltage.

Other than the externally applied potential, there is a built-in potential within this FTJ stack due to the work function difference between the layered materials [132, 133]. The voltage drop due to the built-in potential is defined as [131],

$$\mathrm{V_{built-in}} = \frac{\phi_2 + \phi_\mathrm{c} - \phi_1 - \mathrm{E_{F2}} + \mathrm{E_{F1}}}{\mathrm{e}}, \tag{1.18}$$

where ϕ_1 and ϕ_2 represent the conduction band discontinuities at the top and bottom FE-metal interfaces, respectively. $\mathrm{E_{F1}}$ and $\mathrm{E_{F2}}$ denote the Fermi energies of the top and bottom metallic electrodes, respectively. ϕ_c refers to the band discontinuity at the FE-DE interface and e is the elementary charge. Figure 1.12(c) qualitatively illustrates the built-in voltage distribution across the stack.

The polarization charges in the ferroelectric layer need to be compensated by the M2 electrode in the FE-M2 interface and by the DE in the FE-DE interface. Being a metal, M2 electrode compensates these charges with a Fermi-screening length of δ_2. Whereas the DE will not be able to compensate these charges well, due to the unavailability of charges within. This leads to potential drop across the DE which will be compensated by the M1 electrode with a Fermi-screening length of δ_1. This potential is arising due to the depolarization field within the M1-DE-FE-M2 stack and is shown in Figure 1.12(d) for the two polarization directions. Converting these three potential profiles (applied potential, built-in potential and depolarization potential) into energy profiles and adding it to the energy band diagram of M1-DE-FE-M2 at equilibrium yields energy band diagram shown in Figure 1.12(e) and (f) for the two polarization directions. When the polarization in FE is directed towards the DE, as shown in Figure 1.12(e), the band bending leads to low tunnel resistance. This state is called the ON state. Whereas when the polarization is directed away from the DE, as shown in Figure 1.12(f), the band bending leads to high tunnel resistance. This state is called the OFF state. The details of stack optimization in

M-FE-DE-M FTJ stacks are discussed in Chapter 3.

1.3 FTJs for neuromorphic computing

Neuromorphic computing represents an alternative approach to computing that seeks to emulate the neural structure and function of the human brain. This innovative paradigm aims to overcome the limitations of traditional von Neumann architectures by leveraging the principles of neural networks, where neurons and synapses work together to process and store information concurrently, as shown in Figure 1.13. The two components of the human brain, their functionalities and their artificial counterparts are discussed below.

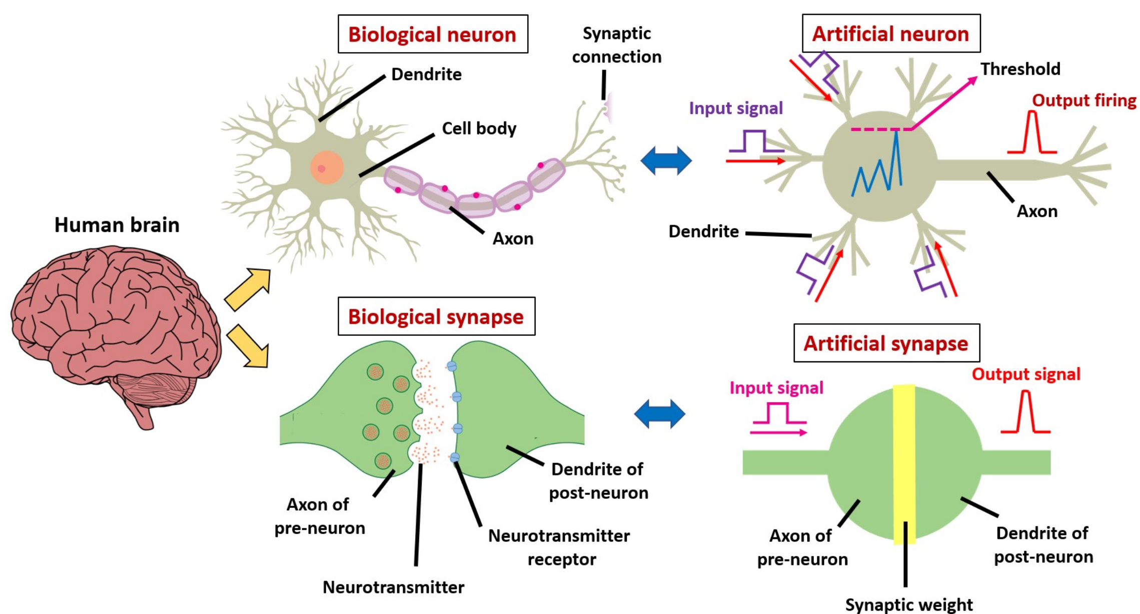

Figure 1.13: Neuromorphic computing is inspired by the human brain, specifically its neurons and synapses. Biological neurons consist of dendrites, somas, and axons. Dendrites collect input signals, which the soma integrates and, if the threshold is exceeded, generates action potentials transmitted along the axons to post-neurons. Synapses connect the axons of pre-neurons to the dendrites of post-neurons, with neurotransmitters facilitating communication. Artificial neurons and synapses in neuromorphic systems aim to replicate these functions. Image of biological neuron adapted from [134].

Neurons:

Neurons are the fundamental units of the brain, responsible for processing and transmitting information through electrical and chemical signals. A neuron consists of three main parts: the cell body, dendrites, and axon. The cell body, or soma, houses the nucleus.

Dendrites extend from the cell body as thin, branch-like structures, creating a tree-like configuration. The axon is a long, slender projection that can extend over a meter in length. The essential function of a biological neuron is to fire an output signal (I_{output}) when the integrated membrane potentials collected from the dendrites exceed a certain threshold. This fundamental behaviour can be simplified into the leaky-integrate-and-fire (LIF) neuron model. In this model, when the input potential from dendrites surpasses the threshold, the neuron generates an output signal. If no signal arrives for an extended period, the information is presumed to gradually decay or leak away over time leading to the recovery of their initial states.

In neuromorphic systems, the structure and function of biological neurons can be mimicked using memristors. In a memristor, the dendrites and axons of a neuron are analogous to the top and bottom electrodes, respectively. The cell body of the neuron corresponds to the active layer of the memristor. When an electrical input pulse (V_{input}) is applied to the top electrode of the memristor, the voltage potential across the device accumulates until it reaches a specific threshold. This accumulation process closely resembles the integration phase of a biological neuron. Upon reaching the threshold, the memristor switches states abruptly, releasing its current (I_{output}) to the bottom electrode. This sudden release mimics the firing action of neurons.

FTJ devices can be utilized to mimic the functionality of neurons [135, 136]. In FTJ devices, the conduction states are stable due to the non-volatile nature of ferroelectric polarization. However, the absence of screening charges at the FE interface can lead to a high depolarization field, causing back-switching of domains and resulting in the decay of the set polarization. By properly controlling the screening charge carrier density, FTJ devices can be converted from non-volatile memories to demonstrate LIF-type behaviour. This was demonstrated in 2019 by Majumdar et al. using a ferroelectric PVDF-based FTJ device with an Nb-doped $SrTiO_3$ substrate [137].

A recent work by Gibertini et al., published in 2022, developed a hybrid FTJ-CMOS Integrate-and-Fire neuron circuit using an HZO-based bilayer FTJ device [138]. This device demonstrated thresholding behaviour in resistance change, which is essential for simulating neuron functionality. The FTJ's accumulative polarization switching, which is defined as polarization switching under identical pulse applications, allows it to integrate

input pulses, mimicking the pulse integration seen in biological neurons. When the integrated input pulses reach a certain threshold, the read current through the FTJ increases and is amplified by the CMOS circuitry, leading to a firing event.

Synapses:

Synapses are the connections between neurons (pre-neuron and post-neuron) that facilitate communication. They play a crucial role in learning and memory by adjusting the strength of synaptic weight (synaptic plasticity) based on neural activity. Plasticity can be categorized into two types based on its stability: long-term and short-term. Long-term plasticity refers to enduring, stable changes in synaptic strength that can last from several minutes to days, and includes long-term potentiation (LTP) and long-term depression (LTD). In contrast, short-term plasticity involves rapidly decaying changes that dissipate within tens of milliseconds to minutes and includes short-term potentiation (STP) and short-term depression (STD). Spike-Timing-Dependent Plasticity (STDP) is a form of synaptic plasticity where the precise timing of pre- and post-synaptic spikes determines the changes in synaptic strength, influencing learning and memory processes [139]. When a pre-synaptic neuron fires shortly before a post-synaptic neuron, the synaptic connection is typically strengthened (potentiation); conversely, if the pre-synaptic neuron fires after the post-synaptic neuron, the connection is weakened (depression).

In neuromorphic computing, artificial synapses are designed to emulate these functions, allowing the system to modify its behaviour based on experience. HZO-based FTJ devices can demonstrate synaptic functionalities by modulating the device resistance through the application of multiple voltage pulses. These pulses can vary in amplitude and width, or they can be identical. Here the polarization switching with sub-switching pulses are utilized to attain intermediate polarization states, which results in the intermediate resistance states of the FTJ devices. In 2018, Chen et. al demonstrated synaptic functionalities like LTP, LTD and STDP with ultra low power HZO-based FTJ device interconnected with hardware neural network [20]. In 2019, Ryu et.al demonstrated LTP, LTD and STDP in FTJ devices with bilayer architecture of p^{+}Si-HZO-Al_2O_3-Ti-Au [121]. Ever since, many researchers have successfully demonstrated synaptic functionalities using HZO-based FTJ devices and this is still an active research area [140–142].

The key feature required for devices to mimic neuron and synapse functionalities is a programmable resistance state. This involves the ability to gradually switch the device's resistance between a high resistance state (HRS) and a low resistance state (LRS) under the influence of electric fields. If the device can exhibit multiple resistance levels between its minimum and maximum values, it can emulate learning processes through synaptic plasticity. In this thesis, we fabricate M-FE-DE-M FTJ devices based on ferroelectric HZO layer. After optimizing the device architecture, we study the impact of electrical programming on the FTJ device performance. We demonstrate multiple resistance states necessary for above mentioned neuromorphic functionalities through pulse programming. The optimized FTJ devices are then integrated to the CMOS back-end of line and the same neuromorphic functionalities are then demonstrated on the CMOS integrated FTJ device.

This research is part of the Horizon 2020 European project "BEOL Technology Platform based on Ferroelectric Synaptic Devices for Advanced Neuromorphic Processors" (BeFerroSynaptic - no. 871737).

Chapter 2

Fabrication and characterization methods

This chapter deals with the intricate processes involved in creating, optimizing, and evaluating FTJ memory devices. It covers various material deposition techniques essential for fabricating FTJ devices, followed by discussions on lithography procedures for electrode patterning. Techniques for assessing layer thickness, structure, and chemical composition are then examined. The process flow for FTJ stack fabrication is outlined, alongside the discussions on electrical measurements for stack characterization. Furthermore, the electrical characterization of different capacitor stacks (with 10 nm HZO) is performed to examine the influence of metal electrodes on the ferroelectric properties.

2.1 Material deposition techniques

Thin film deposition techniques play a pivotal role in the fabrication of electronic devices, offering precise control over the thickness and composition of deposited films. Various methods are employed for thin film deposition, each tailored to specific material requirements and device applications. Physical vapor deposition (PVD) methods involve the conversion of solid material into vapor, which condenses on a substrate to form a thin film. Chemical vapor deposition (CVD) relies on chemical reactions to deposit thin films from gaseous precursors, allowing for conformal coatings with excellent uniformity. The choice of deposition method depends on the specific material properties, device design,

and performance criteria, highlighting the importance of understanding and selecting the most suitable technique for a given application. In this section, we discuss various PVD and CVD techniques, which are used for the fabrication of FTJ devices fabricated and studied in this work.

2.1.1 Atomic layer deposition (ALD)

Atomic layer deposition (ALD) is a thin-film deposition technique which is classified as a subclass of CVD. In ALD, a film is formed on a substrate by exposing its surface to alternate gaseous species, known as precursors or reactants [143, 144]. Here, the precursors are introduced sequentially, not simultaneously. During individual pulses, each precursor undergoes a self-limiting reaction with the surface, ceasing when all available surface sites are engaged. The quantity of material deposited in a single exposure to all precursors (an ALD cycle) is dependent on the interaction between the precursor and the surface. By manipulating the cycle count, it is possible to achieve precise material growth on substrates. In its most basic form, a single ALD cycle involves four steps [144]: (i) exposure of the first precursor, (ii) purge or evacuation of the reaction chamber, (iii) exposure of the second precursor, and (iv) purge or evacuation of the reaction chamber. This cycle is repeated as many times as necessary to obtain the desired film thickness.

ALD offers key benefits, including precise control of film thickness, the ability to coat complex surfaces, and the option to work at lower temperatures. In order to perform ALD successfully, the reaction has to happen at the surface between first and second precursor, hence the surface temperature needs to be high enough for reactions but should not surpass the point where reactants break down [145]. Higher temperatures could lead to breakdown in the gas phase without chemisorption on the surface.

This temperature range is known as the ”ALD temperature window” or simply the ”ALD window”. Operating at too low a temperature results in slow growth due to limited reaction rates, while excessively high temperatures lead to decomposition and rapid growth rates. The typical ALD window for thermal ALD processes is between 150 °C and 350 °C [146].

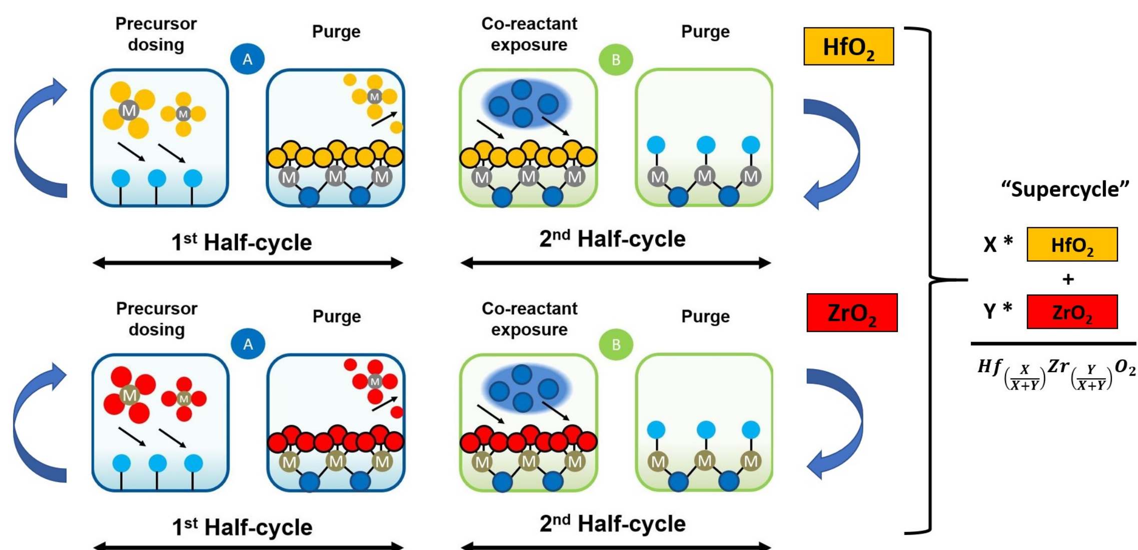

Figure 2.1: The schematic representation of an ALD supercycle for the deposition of $Hf_{0.5}Zr_{0.5}O_2$ layer. An individual ALD supercycle comprises two ALD cycles, one dedicated to HfO_2 and the other to ZrO_2. Each ALD cycle is divided into two parts known as half-cycles, one for the dosing and purging of the appropriate precursor and another for the dosing and purging of the co-reactant. In this case, the co-reactant is water. Figure courtesy: Marco Holzer. Used with permission.

2.1.2 Optimization of ALD deposited ferroelectric Hafnium-Zirconium Oxide

In our research facility, $Hf_{0.5}Zr_{0.5}O_2$ (HZO) thin films were deposited using ALD with an Oxford FlexAl cluster system. This involved alternating depositions of Hf- and Zr-precursors. The development and optimization of the HZO layer using ALD deposition, discussed in this section, were carried out by Mr. Marco Holzer, a former colleague in the same laboratory. The same procedure is applied in the fabrication of HZO based FTJ memory devices, which are extensively examined throughout this thesis.

HZO stands out as a promising choice for Back-End-of-Line (BEOL) applications among various HfO_2-doped systems. Using Zr as a dopant allows achieving ferroelectric properties at lower processing temperatures compared to dopants like Al [114, 147]. The maximum ferroelectric polarization in HZO remains stable at around 50% Zr content, while most other dopants are stable at much lower concentrations (usually $< 20\%$). When it comes to ALD, achieving a uniform solid solution is easier with a 1:1 ratio of HfO_2 and ZrO_2 ALD processes, compared to other ratios [55].

Studies indicate that the ALD process conditions influence the structural and electrical characteristics of HZO layers [69, 148, 149]. If processes are not optimized, there is a risk of increased impurity levels, potentially reducing the endurance and remnant polarization of ferroelectric films in devices [150]. Therefore, the dosing and purging times of the Hf and Zr precursor solutions and for the co-reactant water were first optimized for each compound. The precursors used were Tetrakys-ethyl-methyl-amino hafnium (TEMAH) and Tetrakys-ethyl-methyl-amino zirconium (TEMAZ), heated at 70 °C (TEMAH) and 65 °C (TEMAZ). A schematic representation of an ALD supercycle comprising of two ALD cycles for the deposition of HfO_2 and ZrO_2 layers is shown in Figure 2.1.

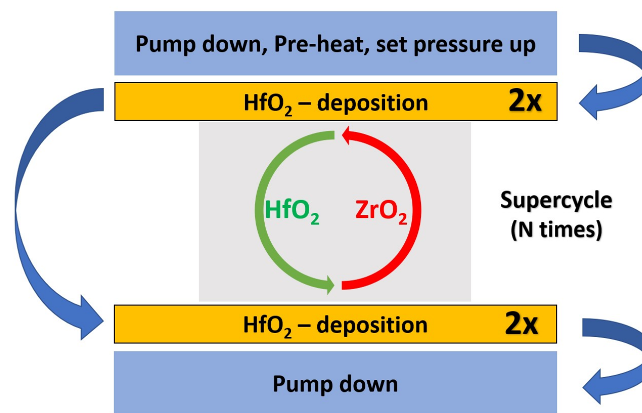

Figure 2.2: Schematic representation of the procedure utilized for the deposition of $Hf_{0.5}Zr_{0.5}O_2$ layer using ALD technique. The process starts by pumping down the system. Then the pressure and the temperature of the system are set to the required values. The deposition starts with 2 ALD cycles of HfO_2 followed by 'N' number of super cycles. Finally, the deposition ends with 2 ALD cycles of HfO_2. In the end, the system is again pumped down. The number of super cycles (N) depends on the desired HZO thickness.

Each ALD cycle contains two half cycles. The first half cycle is for the dosing and purging of the precursors, TEMAH in case of HfO_2 and TEMAZ in case of ZrO_2. Whereas the second half cycle is for the dosing and purging of the water co-reactant. For attaining a ratio of 1:1, one HfO_2 cycle is followed by one ZrO_2 cycle. Each film deposition is started and ended with two cycles of Hafnia as shown in Figure 2.2 [151]. A common ALD window was determined at 250 °C as shown in Figure 2.3(a) for TEMAH and TEMAZ precursors. The optimized parameters for the two precursors are summarized in Table 2.1. The growth per cycle (GPC) for HZO layer deposited by this optimized parameter is 0.149 nm/cycle as shown in Figure 2.3(b).

Using spectroscopic ellipsometry, we not only determined the film thickness but also

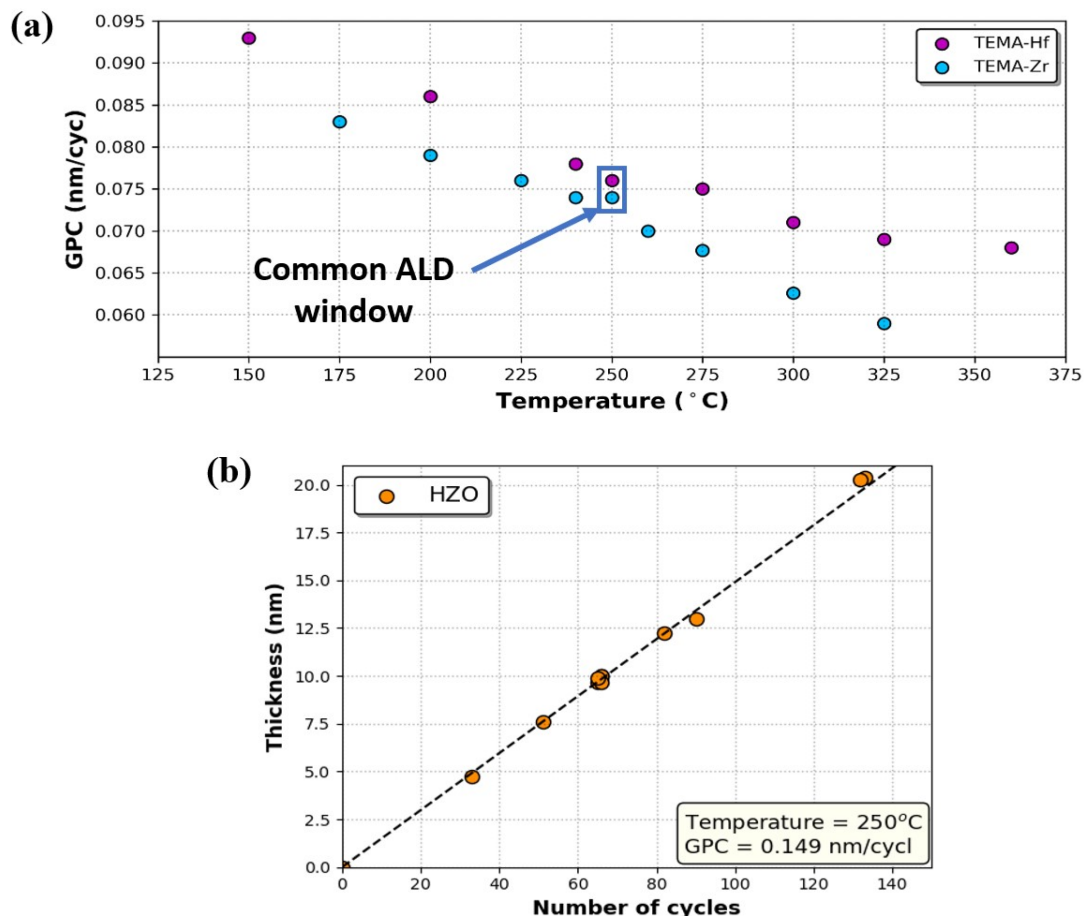

Figure 2.3: (a) Temperature vs GPC graph corresponding to TEMA-Hf and TEMA-Zr precursors. This indicates the temperature stability of the two precursors. A common ALD window is obtained at 250°C where both the precursors show a GPC value of ∼0.075 nm/cycle. (b) Number of cycles vs thickness graph corresponding to the HZO layer deposited with the optimized parameters shown in Table 2.1 and procedure discussed in Figure 2.2. Here the number of cycles represent the number of super cycles 'N', marked in Figure 3.2. Figure courtesy: Marco Holzer. Used with permission.

analyzed their composition through an effective medium approach, along with their optical index. The average composition was identified as $Hf_{0.54}Zr_{0.46}O_2$. Across a 4-inch wafer, the film thickness showed a 7% variation for a 9 nm thick film. The refractive index was measured at 2.03, and X-ray reflectometry confirmed a density of 6.2 g/cm^3, aligning well with existing literature values [68]. X-ray diffraction confirmed that the HZO films, as deposited, are in an amorphous state.

Precursor	Dosing time precursor	Purging time precursor	Dosing time water	Purging time water
TEMA-Hf	700 ms	10 s	40 ms	60 s
TEMA-Zr	1100 ms	10 s	50 ms	90 s

Table 2.1: Optimized parameters for TEMAH and TEMAZ precursors.

2.1.3 Sputter deposition

Sputter deposition is a form of PVD which utilizes the sputtering phenomenon for the deposition of thin films. Sputtering relies on utilizing the energy of a plasma (partially ionized gas) directed onto the surface of a target (cathode). As a result of high-energy ions colliding with atoms in the target material, there is a transfer of momentum between them [152]. If, upon reaching the target surface, the ion's energy exceeds the bonding energy between the atoms of the target material, the collided atom detaches from the target material [153]. Figure 2.4 illustrates a schematic depiction of the sputter deposition technique. The sputtering process systematically extracts individual atoms from the target material, depositing them one by one onto the substrate (anode). To achieve this, a plasma is generated by ionizing an inert gas, typically Argon, using a potential difference. This plasma consists of Ar+ ions that are accelerated and contained around the target, facilitated by the presence of an electric field.

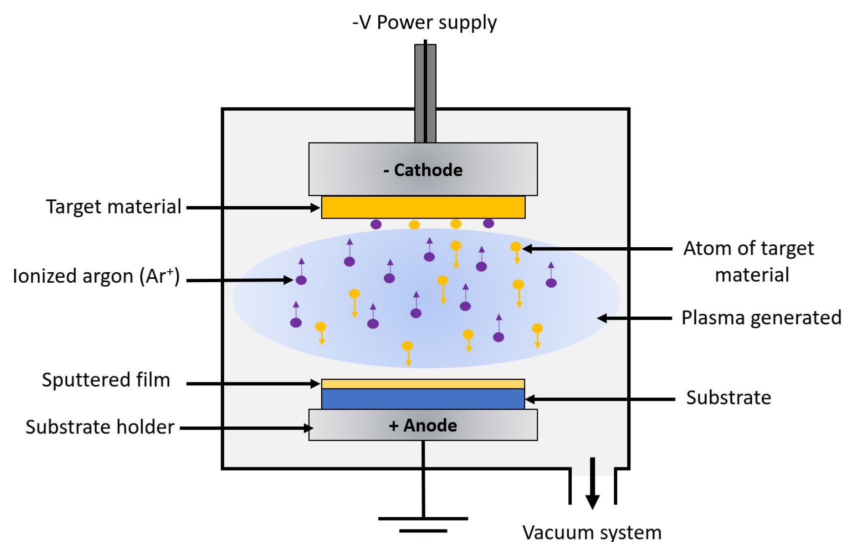

Figure 2.4: A schematic representation showing the standard sputtering technique.

The number of atoms ejected or "Sputtered off" from the target or source material is

called the sputter yield. The sputter yield is influenced by several key factors. The angle at which ions impinge upon the target material's surface plays a significant role. Additionally, the sputter yield is affected by the energy carried by ions during collisions, the mass of both ions and atoms in the target material, and the binding energy between the atoms of the target material [154]. Moreover, the plasma gas pressure in the system serves as another essential factor in shaping the efficiency of the sputtering process by influencing the deposition rate, film quality and uniformity. The interplay of these elements determines the effectiveness and reliability of thin film deposition through sputtering. In this thesis, the Tungsten (W) and Titanium nitride (TiN) metals, utilized as device electrodes, are deposited via sputtering deposition at room temperature.

2.1.4 Thermal evaporation

Thermal evaporation functions by evaporating source material within a vacuum at high temperatures facilitating the movement of vapor particles to substrate directly and solidify once more [155]. In order to attain the high melting points required for metals, a significant direct current (DC) is applied to heat the resistive boat (crucible) containing the target material. This process is facilitated by maintaining a high vacuum (below 10^{-4} Pa) to enable the evaporation and deposition of metal onto the substrate, as illustrated in Figure 2.5.

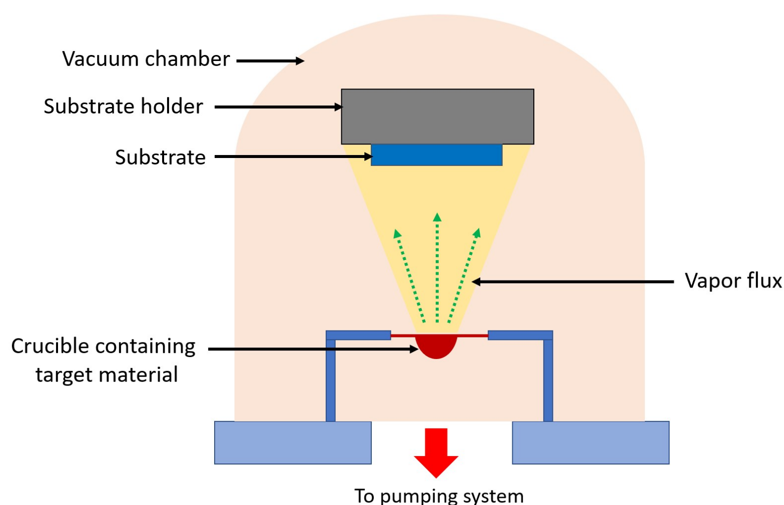

Figure 2.5: A schematic representation of the thermal evaporation process [156].

This approach is particularly suitable for materials with lower melting points. The rate

of evaporation depends on the vapor pressure of the source material at the evaporation temperature. By applying Joule heating to a standard Tungsten or Molybdenum crucible, temperatures of up to 2800 K can be achieved, resulting in significant vapor pressures for most metals [157, 158]. In this thesis, the top electrode of certain FTJ devices underwent patterning through a Titanium (Ti, 10 nm)/Gold (Au, 100 nm) lift-off process (explained in section 2.2), followed by a wet etch of the top metal layer. The deposition of Ti and Au was achieved using a thermal evaporator.

2.1.5 Electron beam (E-beam) evaporation

Electron beam (E-beam) evaporation is a physical vapor deposition method where high-energy electrons, in the form of an intense beam, are used to evaporate the source material [155]. A hot filament causes the thermionic emission of electrons. The electron beam gains high kinetic energy and is directed towards the target material with the help of a magnetic field as shown in Figure 2.6. The kinetic energy transforms into thermal

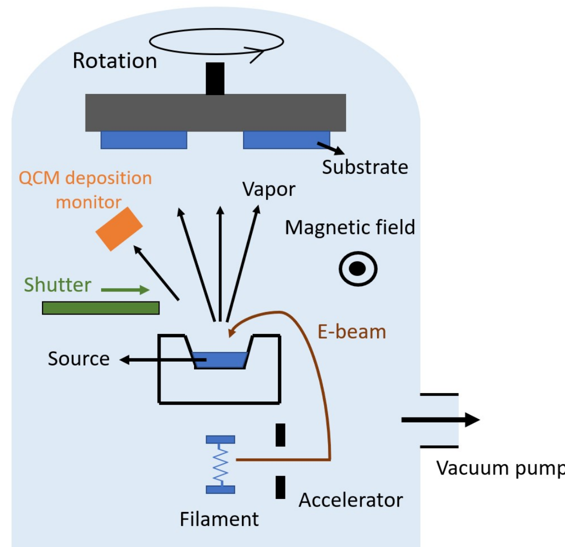

Figure 2.6: A schematic representation of E-beam evaporator [159].

energy, raising the surface temperature of material, causing evaporation and deposition onto the substrate. The deposition rate relies on the target material and E-beam power. The thickness of the deposited film can be measured in real-time using a quartz crystal monitor. To prevent the filament from melting due to the incoming evaporant, it is positioned away from its direct path [155, 159]. The electron beam is guided towards the

surface of substrate through a magnetic field. In this thesis, the top electrode of certain FTJ devices underwent patterning through a Ti(10 nm)/ Platinum (Pt, 100 nm) lift-off process, followed by a wet etch of the top metal layer. The deposition of Ti and Pt was achieved using a E-beam evaporator due to the high melting point of Pt.

2.2 Lithography

Lithography is a process that enables the precise and repetitive creation of a specific pattern in a specialized material layer (resist) on a substrate by inducing a chemical modification [160]. In general, this pattern is then transferred to another functional layer using etching or lift-off process [161]. The lithography process typically comprises of the following steps:

1. **Sample cleaning**:- The sample needs to be thoroughly cleaned, and most impurities such as organic materials or dust particles can be eliminated by rinsing it with acetone or isopropanol in an ultrasound bath. To remove surface water, it is beneficial to dry the sample for one minute at 100°C when surface is not a metal that gets quickly oxidizes due to heating, facilitating better wetting of the surface by the resist.

2. **Resist coating**: Resists, also known as photoresists, are composed of resin (acting as a binder that provides physical properties like adhesion and chemical resistance), sensitizer (containing a photoactive compound), and solvent (maintaining the resist in liquid form). The sensitizer component alters the resist's chemistry upon exposure to light, affecting its solubility. When selecting a resist, compatibility with solvents, working temperatures, and processes must be considered. There are two types of resists available: positive and negative. Positive photoresist becomes soluble in the developer solution wherever exposed to light, while negative photoresist becomes resistant to dissolution in the developer wherever exposed to light. In order to coat a sample with resist, it is placed at the center of a spin coater's rotary holder, fixed in position using vacuum, and a small amount of resist is dispensed onto the sample surface. A spin coater spreads the resist evenly, with the time duration, acceleration, and rotation speed determining the thickness and uniformity of

the resist film. One must be careful not to dispense too much resist, as excess may cause resist to leak outside the sample and hinder uniform coating. One drawback of spin coating is that it results in a bulge around the border also called edge bead, rendering it unusable for very small samples (smaller than $1 \times 1\ \mathrm{cm}^2$).

3. **Annealing**: A resist possesses a sufficient level of viscosity which facilitates easy coating. During the annealing step, the resist undergoes a controlled heating process to ensure the removal of solvents, leading to the establishment of a stable and well-prepared film where only photoactive compound and binder are left behind. This preliminary treatment is crucial for enhancing the overall quality and performance of the resist layer before subsequent processing steps.

4. **Exposure**: The exposure of light is a key element in the creation of patterns on the resist material by changing its chemistry. The exposure process can be accomplished using advanced tools such as a photolithography tool or a laser lithography tool, both of which will be discussed in detail later in this section. This crucial step plays a fundamental role in determining the precision of the resulting patterns.

5. **Development**: The resist is paired with a developer solution. In case of positive resist, the polymerized region of the resist becomes soluble in the developer solution and the resist region which is not exposed to the light remains insoluble. The resolution of the patterns is determined by factors like developer concentration, mechanical agitation, and development time. The development process concludes by rinsing the sample in a separate solution. Distilled (DI) water is typically used for this purpose.

Once the resist is developed, a pattern is obtained on the resist layer. In order to transfer this pattern to the thin layer residing underneath the resist layer, etching process needs to be performed. Etching can be done in two different ways. One is ‘wet etching’, in which a chemical solution is used to remove the material from the sample surface where the resist coating is not present. Wet etching involves immersing the substrate in a chemical solution, known as an etchant, which reacts with the exposed material, resulting in its dissolution. The choice of etchant depends on the material to be removed. This method is particularly suitable for isotropic etching, where material is to be removed

uniformly in all directions. The second way is ‘dry etching’. Unlike wet etching, it involves the removal of material from a substrate using reactive gases in a plasma state. This method offers greater control and precision, allowing for anisotropic etching with well-defined patterns. Dry etching is advantageous for creating intricate structures and achieving high aspect ratios [162]. Dry etching is favored for its ability to achieve fine feature sizes and better selectivity between materials. Reactive ion etching (RIE) is a dry etching technique which employs anisotropic ion bombardment. This involves chemical reactions in a plasma environment.

Lithography can be utilized to pattern the layer intended for deposition, a process known as the ’lift-off technique’. Here, material deposition occurs on a substrate with a patterned resist layer. The material is deposited both on the substrate where the resist is absent and on top of the resist where it is present. After deposition, the resist is removed using Acetone and Isopropanol in an ultrasound bath. This step removes the resist from the substrate surface, along with any material deposited on top of the resist. What remains are the substrate and the material deposited only in the areas where the resist was absent.

As discussed earlier, expose to light of resist material is of prime importance in the creation of patterns. For this purpose, two tools are used as discussed below:

2.2.1 Photolithography

In photolithography, a photomask (a plate with microscopic patterns) is used to transfer a desired pattern onto a photoresist layer on a substrate when exposed to ultraviolet light [163]. The light triggers a chemical reaction in the photoresist layer on the substrate placed below the photomask as shown in Figure 2.7. For positive photoresists, the exposed areas become soluble in the developer solution, while for negative photoresists, they become insoluble. This creates a pattern on the substrate. The photolithography process was carried out using an MA6 mask aligner with a light wavelength of 350 nm.

2.2.2 Laser lithography

Laser lithography, also known as mask-less lithography, offers an alternative to traditional photolithography without the need for photomasks. Patterns are created using a layout

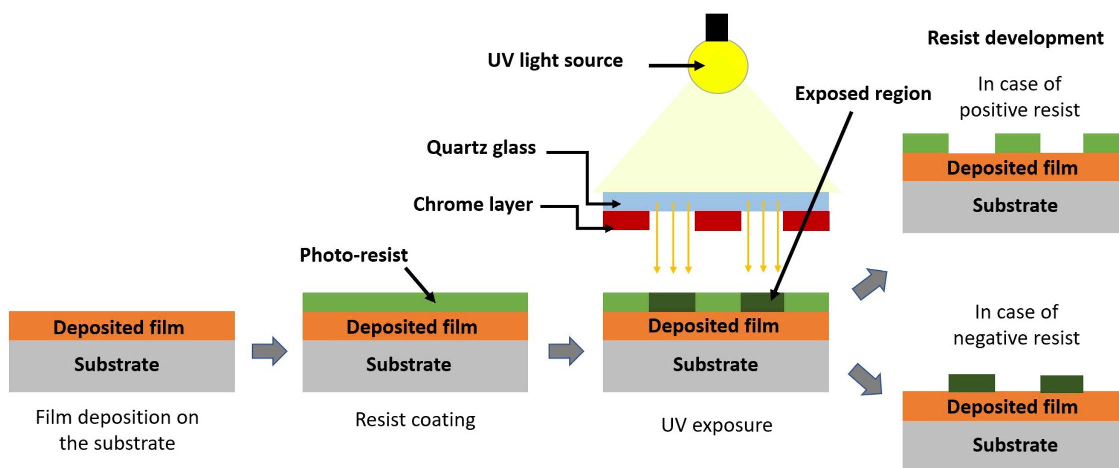

Figure 2.7: A schematic representation of different steps involved in photolithography.

editing software. In this thesis, KLayout[1] was used. These designs are then transferred to the laser lithography software, which directly exposes a laser beam onto the substrate surface using a spatial light modulator. Since there is no reliance on photomasks, modifications to the designs can be made easily, allowing for immediate lithography without waiting. This process is straightforward where one just loads the design into the software and begins the exposure process. The laser beam exposure leads to a chemical reaction on the photo resist. This reaction renders specific areas either soluble or insoluble in the developer solution, creating the pattern on the substrate. The laser lithography was performed using the 'Heidelberg Instruments DWL 66+' laser writer.

2.3 Thickness, structural, and chemical analysis

Thin films deposited through different deposition techniques, as discussed in the previous section, need to be analyzed to understand the film thickness, structural and chemical composition. For the fabrication of FTJ devices, it is crucial to optimize the properties of the individual thin film components. In our study, the thicknesses of the layers are measured with the help of spectroscopic ellipsometry measurements. The crystallographic structures of the materials are analyzed with the help of X-ray diffraction (XRD) technique. The chemical compositions of the individual layers are analyzed with the help of X-ray photoelectron spectroscopy (XPS). These techniques are discussed in detail below.

[1]https://www.klayout.de/

2.3.1 Ellipsometry

Ellipsometry is an optical technique widely used for characterizing thin films and material properties on the surfaces [164]. It measures changes in the polarization state of light upon reflection or transmission through a sample and compares it with different models. An electromagnetic radiation is emitted by a light source and it is polarized by a polarizer (shown in Figure 2.8). It can pass through an optional compensator and then it falls on the sample surface at an incident angle. The change in the polarization of light upon reflection depends on the properties of the sample such as thickness (t), complex refractive index ($\tilde{n}$) or the complex dielectric function (ϵ) [165, 166]. The complex refractive index is defined as

$$\tilde{n} = n + ik. \tag{2.1}$$

The real part of $\tilde{n}$ in Eq. (2.1), which is simply called the refractive index (n) affects the wavelength of light (λ) when it passes from one medium to the other. The imaginary part of the complex refractive index, k, is known as the extinction coefficient. The amplitude of the electromagnetic wave decreases with the increase in k value. The absorption coefficient (α), a measure of the rate at which the intensity of electromagnetic radiation decreases as it passes through a particular substance, is related to the extinction coefficient and wavelength by the following equation

$$\alpha = \frac{4\pi k}{\lambda}. \tag{2.2}$$

The penetration depth (ζ), which is the distance from the surface of the material at which the light intensity has decreased to I_0/e, where I_0 is the initial intensity and e is the Euler's number is defined as

$$\zeta = \frac{1}{\alpha}. \tag{2.3}$$

The intensity of light inside the material at distance z in the direction of propagation of light is calculated by the following equation

$$I(z) = I_0 \, e^{-\alpha z}. \tag{2.4}$$

The complex refractive index is related to the complex dielectric function by the following relation

$$\tilde{n} = \sqrt{\epsilon} = \sqrt{\epsilon_1 + \epsilon_2} \tag{2.5}$$

where $\epsilon_1 = n^2 - k^2$ and $\epsilon_2 = 2nk$.

Since the nature of the sample surface influences the properties of the reflected light, the light which is reflected from the sample surface is different from the light which was incident on the sample. The reflected light passes through an optional compensator and a polarizer (which we call the analyzer) and reaches the detector. The incident angle and the reflected angles are equal. The plane through which the incident beam (i) and the reflected beam (r) pass through is called the plane of incidence. Light polarized parallel to this plane is referred to as p-polarized, while a polarization direction perpendicular to the plane of incidence is termed s-polarized. The detector quantifies the complex reflectance ratio, denoted as ρ, for a system. This ratio can be expressed in terms of the amplitude component (Ψ) and the phase difference between p and s polarized light (Δ).

$$\rho = \frac{r_p}{r_s} = \tan(\Psi) e^{i\Delta} \tag{2.6}$$

In this context, r_p and r_s represent the Fresnel reflection coefficients for p-polarized and s-polarized light, respectively, constituting the complex reflection coefficients of the sample for the respective polarizations. They are defined as the ratio of the reflected to incident electric fields corresponding to their specific polarizations.

$$r_p = \frac{E_{rp}}{E_{ip}}, \quad r_s = \frac{E_{rs}}{E_{is}} \tag{2.7}$$

In ellipsometry, the measured parameters Ψ and Δ cannot be directly translated into the optical constants of the sample. Typically, it requires fitting of models to the measured data. In order to find the film thickness of the deposited film using ellipsometry, we start by assuming a model. The model is chosen by considering the number of layers and the layer type (isotropic, anisotropic or graded) [167]. The next step is to determine or

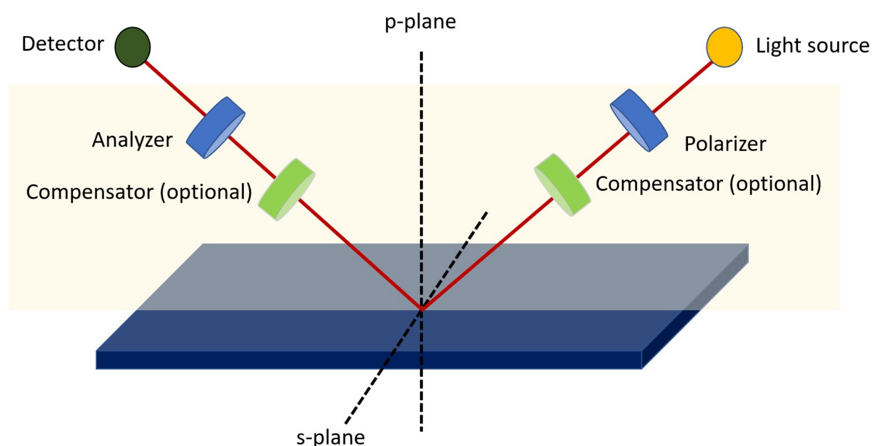

Figure 2.8: Schematic of the ellipsometry setup. Unpolarized light emitted from a light source is polarized by passing through a polarizer. It then reflects off the surface of a sample, passes through an analyzer, and ultimately reaches a detector.

parametrize the optical parameters of each layer. An optical spectra is then constructed based on the estimated optical parameters and this is fitted analytically with the experimental data using a suitable algorithm. For attaining reasonable value from the fitting, it is crucial to start with a reasonable starting parameter. If the figure of merit indicates a bad fit, the fitting needs to be repeated. The spectroscopic ellipsometry model used for measuring the film thicknesses was developed by Dr. Florian Maudet, a postdoctoral fellow at QM-IFOX, HZB.

2.3.2 Grazing incidence X-ray diffraction (GIXRD)

X-ray diffraction (XRD) is a non-destructive technique for determining the atomic and molecular structure of materials. This method involves diffracting X-rays through the material under examination, as shown in Figure 2.9(a). The X-rays, which are short-wavelength electromagnetic waves, interact with the electrons of the atoms in the sample. This interaction results in constructive and destructive interference patterns, which are detected and analyzed to determine the crystallographic properties of the material.

In a crystalline material, atoms are arranged in a regular three-dimensional distribution in space, as depicted in Figure 2.9(b). This arrangement gives rise to the formation of parallel planes separated by a distance denoted as d_{hkl}, which is material-dependent. When a monochromatic X-ray beam with a specific wavelength (λ) is directed at a crystalline material at an angle (θ), diffraction takes place if the path length travelled by the

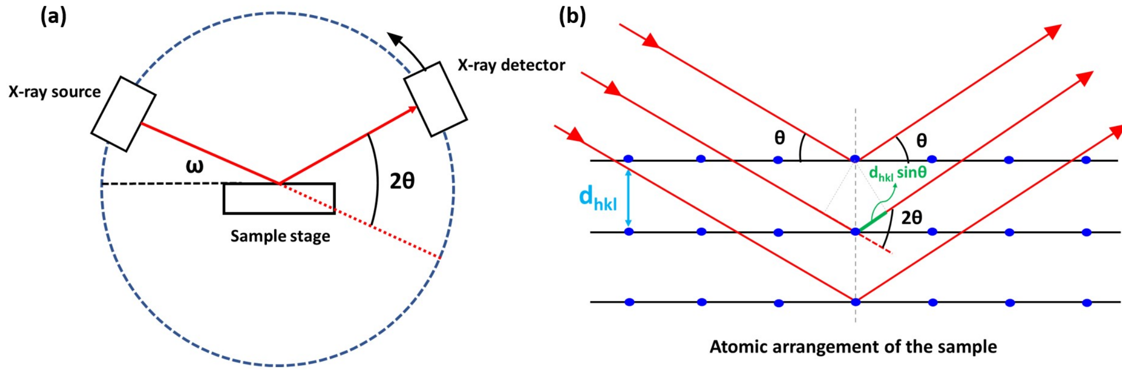

Figure 2.9: (a) Schematic diagram of XRD measurement set-up. The X-ray tube emits a ray that is initially diffracted by the sample and subsequently collected by the detector. (b) Schematic representation of Bragg's law.

X-rays, as they are successively reflected from crystal planes, correspond to an integer (n) multiple of the wavelength, in accordance with Bragg's law [168, 169]. The resulting pattern of angular positions and intensities of the diffracted peaks serves as a characteristic feature for the sample. Bragg's law is mathematically defined as:

$$2\, d_{hkl}\, \sin\theta = n\lambda \tag{2.8}$$

In the traditional XRD technique, the X-rays can penetrate deeper than the thickness of the film. Thus, the resulting diffraction pattern may include undesirable substrate peaks and background noise. Hence, in order to analyze thin films using XRD, it is crucial to minimize the substrate signal. Grazing Incident X-ray Diffraction (GIXRD) enhances the diffraction from the film layer by minimizing the angle of incidence to a smaller value, typically ranging from 0.5° to 1° [170]. GIXRD proves valuable for phase analysis of crystalline thin films, especially those with a thickness below 100 nm.

GIXRD spectra of p^+Si-TiN (30 nm)-HZO (10 nm)-TiN (30 nm) stack before and after the crystallization of HZO with an incident angle of 1° is shown in Figure 2.10. Here, the crystallization of HZO is performed using rapid thermal processing (RTP) anneal at different temperatures (400 °C, 450 °C and 600 °C) in N_2 atmosphere. The TiN top electrode was removed by wet etching with SC1 solution at 50 °C before the XRD measurement. This step is required for attaining more intensity from the diffracted peaks corresponding to the HZO layer. The spectra (Figure 2.10) show peaks corresponding to orthorhombic (o) and tetragonal (t) phases of HZO, indicating the presence of these

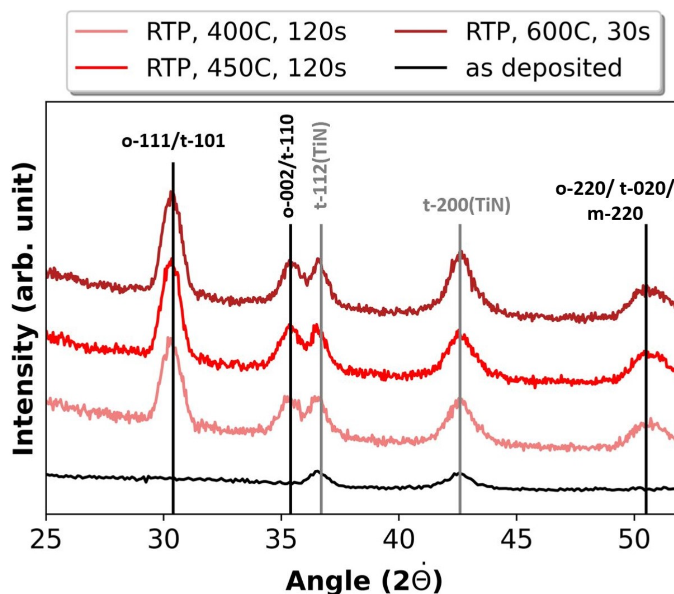

Figure 2.10: GIXRD measurement on p^+Si-TiN (30 nm)-HZO (10 nm)-TiN (30 nm) stack before and after the crystallization anneal at different temperatures. The top TiN electrode was removed by etching with SC1 solution. Figure courtesy: Marco Holzer. Used with permission.

phases in the sample after crystallization anneal, confirming the polycrystalline nature of the HZO layer [71, 171, 172]. The spectra also show peaks corresponding to the TiN bottom electrode. A comparison between the XRD spectra of the as deposited film (before the crystallization anneal) and after the crystallization anneal confirms that the HZO layer shows the presence of orthorhombic phase only after the annealing process. Because the diffraction peaks corresponding to orthorhombic and tetragonal phases are closely positioned, it is not possible to distinguish them. Since the low-temperature annealing process (400 °C) indicates the presence of ferroelectric orthorhombic phase, the annealing condition for the FTJ devices are fixed to 400 °C, owing to its compatibility with CMOS technology.

2.3.3 X-ray photoelectron spectroscopy (XPS)

X-ray photoelectron spectroscopy (XPS) serves as a non-destructive, surface-sensitive, quantitative spectroscopic method, which provides information about the chemical and electronic state of occupied electronic orbitals in the material. It relies on the photoelectric effect, where the absorption of light with adequate energy ejects electrons from both core and valence energy levels, reaching energies high enough to exit the sample. These

emitted electrons, known as photoelectrons, are analyzed based on their kinetic energy, which is directly linked to the chemical and electronic state of the emitting atom.

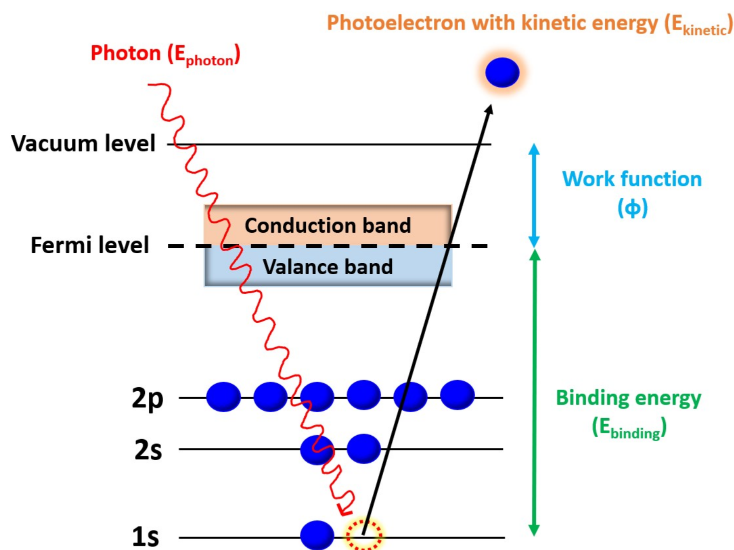

Figure 2.11: Schematic illustration of the core-level photoelectron emission by the photoelectric effect in a metal. This figure is adapted from ref [173]

The essential components of an XPS instrument include an X-ray source, an ultra-high vacuum (UHV) chamber, a hemispherical electron energy analyzer, and a detector. The X-ray source typically employs monochromatic X-rays, often generated by a focused X-ray beam, to ensure accurate and specific excitation of the sample. When a sample is bombarded with X-rays of sufficient energy, inner-shell electrons are ejected from the atoms, as shown in Figure 2.11. The emitted electrons are then directed by electrostatic lenses to the entrance of an energy analyzer. Ultra-high vacuum ($\sim 10^{-10}$ mbar) environment is used to ensure a negligible loss of the electron kinetic energy. Inside the hemispherical analyzer, the electrons are then deflected using a radial field, allowing only electrons with certain energy (called pass energy) to be able to reach the detector. This process allows production of a detailed spectrum that reveals the chemical and electronic characteristics of the material under investigation [173].

By leveraging the known energy of X-rays with a specific wavelength (e.g., for Al K_α X-rays, E_{photon} = 1486.7 eV) and measuring the kinetic energies of emitted electrons, the binding energy of each electron can be calculated using the photoelectric effect equation:

$$E_{binding} = E_{photon} - (E_{kinetic} + \phi) \tag{2.9}$$

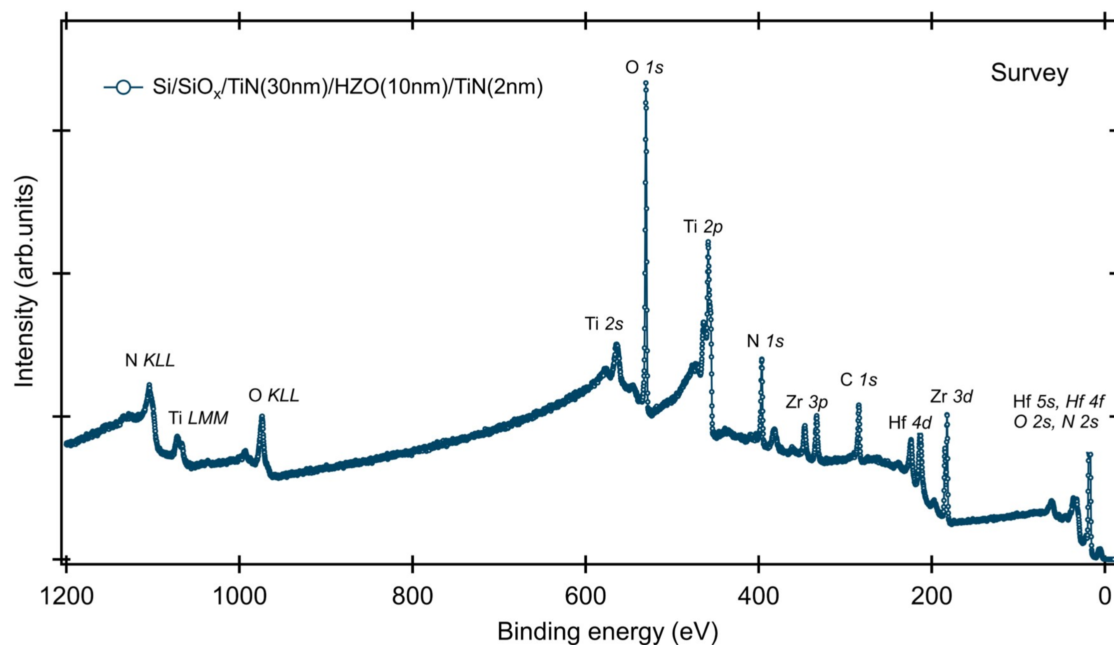

Figure 2.12: XPS measurement on TiN (30 nm)-HZO (10 nm)-TiN (30 nm) stack annealed in RTP at 400 °C. The top electrode undergoes in-situ Ar+ sputtering for etching, leaving behind only a 2 nm layer of TiN in place of the original top electrode. Figure courtesy: Dr. Wassim Hamouda (postdoc fellow at QM-IFOX, HZB). Used with permission.

Here, $E_{binding}$ represents the electron's binding energy measured relative to the Fermi level, E_{photon} is the energy of the X-ray photons and $E_{kinetic}$ is the electron's kinetic energy as determined by the instrument. These are shown in Figure 2.11. The term ϕ is work function of the material's surface. In actual measurements, this term is a constant that typically requires minimal adjustment. The NIST database is equipped with tables of binding energies, showing the shell and spin-orbit of each peak associated with a specific element [174, 175]. Given that these experimentally determined energies are distinctive to particular elements, they serve as a direct means to identify peaks in materials with unknown elemental compositions.

XPS spectra from a TiN (30 nm)-HZO (10 nm)-TiN (30 nm) stack, after RTP anneal at 400 °C is shown in Figure 2.12. Here, the top electrode is etched using in-situ Ar+ sputtering and only 2 nm TiN is remaining in place of top electrode. This step is vital for increasing the intensity of emitted electrons from the HZO layer beneath the TiN top electrode. This is achieved by reducing the inelastic mean free path of the ejected electrons, facilitated by laboratory X-ray sources. Hard X-rays (>2 keV) generated from synchrotron radiation can be an alternative to measure effective XPS signal through thick and

realistic top electrodes (e.g 30 nm). This variety of XPS technique is called hard X-ray photoelectron spectroscpy (HAXPES). The spectrum (in Figure 2.12) displays characteristic peaks corresponding to the elements present, notably Titanium (Ti), Nitrogen (N), Hafnium (Hf), Zirconium (Zr), and Oxygen (O). The TiN layers exhibit prominent peaks indicative of Ti 2p and N 1s core levels, illustrating the presence of Ti-N bonds. In the HZO layer, peaks related to Hf 4f, Zr 3d, and O 1s core levels are observed, suggesting the presence of hafnium, zirconium, and oxygen atoms in various oxidation states [176]. Using the relative intensities of the peaks and the so-called residual standard factors (RSF), one can estimate the stoichiometry of the analyzed film. The result indicate the desired nominal stoichiometry of 1:1 between Hf and Zr. The XPS measurement and the data analysis are performed by Dr. Wassim Hamouda.

2.4 Device fabrication process flow

The FTJ devices examined in this study feature a ferroelectric HZO layer approximately 10 nm thick and a dielectric Al_2O_3 layer ranging from 1 to 3 nm in thickness, sandwiched between two metal electrodes. These devices are fabricated on a p+-doped Si wafer with a resistivity of $\sim$ 0.005 Ωcm. To facilitate work in our laboratory, we cut the Si wafer and work with substrates measuring roughly 2$\times$2 cm^2. In this session, we look into the three distinct process flows utilized for the fabrication of FTJ devices.

2.4.1 Blanket bottom electrode and lift-off top electrode

A relatively simpler method for fabricating the FTJ device involves utilizing a blanket bottom electrode and depositing the top electrode through a lift-off process, depicted in Figure 2.13. In this approach, the top electrode undergoes patterning while the bottom electrode remains unpatterned. In order to establish electrical connectivity with the bottom electrode, one must access it through the underside of substrate (through the chuck). As illustrated in the Figure 2.13, the fabrication process begins with substrate cleaning using Acetone, facilitating the removal of organic impurities. This is followed by Isopropanol cleaning, ensuring the elimination of contaminated Acetone residue or streaks. Subsequently, the substrate is immersed in a 1% Hydrofluoric acid (HF) solution to re-

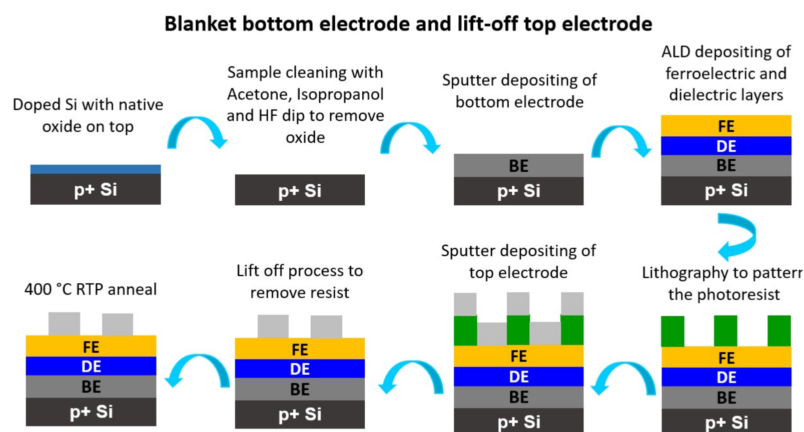

Figure 2.13: Schematic representation of the process flow to fabricate FTJ devices with blanket bottom electrode and lift-off top electrode.

move the native oxide (SiO_2) from the surface. After rinsing with DI water and drying with N_2 blow dry, the bottom electrode (BE) is deposited onto the prepared substrate through sputtering deposition at room temperature. The dielectric (DE) layer is then deposited via ALD deposition at 250 °C, employing trimethylaluminium (TMA) precursor and water as a co-reactant for oxidation. Then, the ferroelectric (FE) layer is deposited using ALD, as discussed in Section 2.1.2. Lithography is then conducted on this sample to pattern the photoresist, followed by sputter deposition of the top electrode (TE). During the lift-off process, the photoresist is removed using Acetone and Isopropanol cleaning. The sample then undergoes annealing in RTP at 400 °C, 120 s in N_2 ambient for HZO crystallization. This method can also be employed for fabricating Metal-Ferroelectric-Metal (M-FE-M) structures, wherein only the FE layer needs ALD deposition, excluding the DE layer. However, a limitation of this process flow is in its applicability only when the dielectric Al_2O_3 layer is positioned near the bottom electrode. The developer (AZ 726 MIF developer, tetramethylammonium hydroxyde) solution used in the lithography process lacks selectivity towards the Al_2O_3 layer, thus employing this technique when the Al_2O_3 layer is near the top electrode could result in unwanted etching of the Al_2O_3 layer from the device area.

2.4.2 Blanket bottom electrode and top electrode patterned by etching

In order to overcome the limitation of patterning top electrode through lift-off process, we use the following process flow for the fabrication of FTJ devices. Thus, this technique can be used in both cases where the dielectric is placed near the bottom electrode as well as near the top electrode. As the bottom electrode is not patterned, similar to previous case, the electrical connection to the bottom electrode is made through the chuck. So the fabrication steps remain similar to the process flow discussed previously until the ALD deposition of the FE and DE layers. After the ALD deposition, TE is deposited through sputtering deposition as a blanket layer, as shown in Figure 2.14. The sample is then annealed in RTP at 400°C for HZO crystallization.

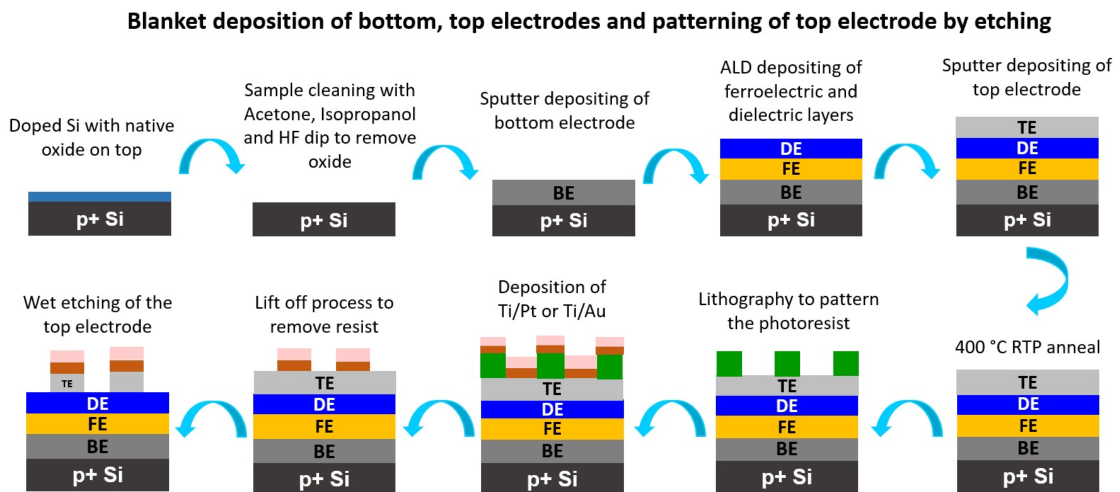

Figure 2.14: Schematic representation of the process flow to fabricate FTJ devices with blanket bottom electrode and top electrode patterned by etching.

The next step is to do lithography to pattern the photo resist and etch the top metal from everywhere other than the device area. However, the resist delaminated when the sample was immersed in the wet etching solutions. Therefore, a hardmask was necessary to etch the top electrode. Lithography followed by lift-off of Ti(10 nm)/Au(100 nm) deposited through thermal evaporation or Ti (10 nm)/Pt (100 nm) deposited through e-beam evaporation was performed on top of the top electrode. The Ti layer helps to increase the adhesion between the Au or Pt metal and the top electrode. This capping layer does not impact the FTJ device performance as the resistance of these layers are very small ($\sim$ few

Ω) compared to that of the FTJ device (∼ GΩ). The wet etching solutions (SC1 solution at 50 °C in case of TiN metal and 30% H_2O_2 solution at 50 °C in case of W metal) are selective to these capping metals and thus it is possible to wet etch the top electrode from region outside the device area this way.

2.4.3 Patterned bottom and top electrodes

The primary objective of this thesis is to integrate FTJ devices with CMOS chips. In order to achieve this goal, it is important to pattern the bottom electrodes of the FTJ devices. Applying a uniform layer of metal atop the CMOS chip would render the circuits and transistors inaccessible. This section discusses the process flow employed to fabricate bottom electrode patterned FTJ devices. As both the bottom and top electrodes will be patterned in this scenario, electrical contacts can be directly established. Hence, it becomes essential to fabricate the devices on a dielectric platform to prevent short circuits between them. Thus, a p+ doped Si wafer coated with a 300 nm layer of SiO_2 serves as the substrate for the fabrication of bottom electrode patterned FTJ devices.

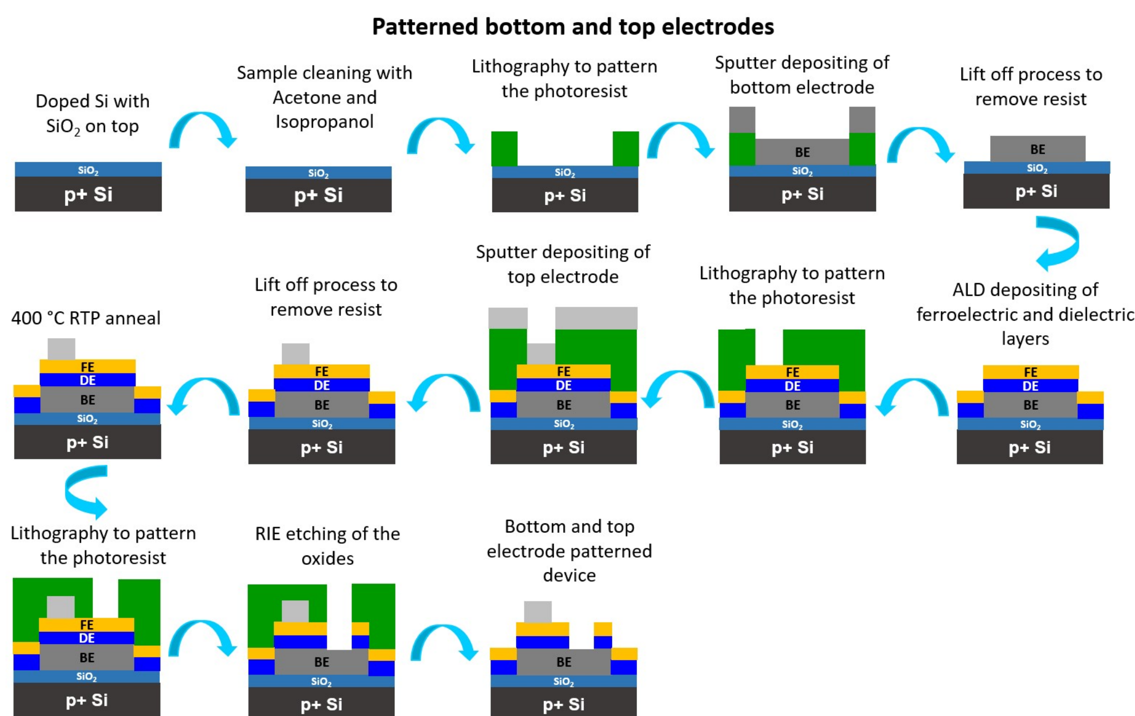

Figure 2.15: Schematic representation of the process flow used for fabricating bottom and top electrode patterned FTJ devices.

As shown in Figure 2.15, the fabrication process starts with the sample cleaning with

Acetone and Isopropanol. Here HF dip is not performed because of the presence of SiO_2 which is necessary for the electrical isolation of the FTJ devices. The bottom electrode undergoes patterning via lithography, followed by sputter deposition and a lift-off process. Subsequently, ALD is employed to deposit dielectric and ferroelectric layers onto the sample. The top electrode is then deposited using lift-off process. At this stage, crystallization anneal is carried out using RTP. Following the anneal, lithography is conducted to pattern the photoresist for the RIE etching (with BCl_3) of oxides from the bottom electrode contact region. This process facilitates direct electrical contact to the bottom electrode.

2.5 Electrical Characterization

In this section, we describe the electrical measurement techniques used to characterize the FTJ devices studied in this work.

2.5.1 Polarization-Voltage (P-V) measurement

The polarization-voltage (P-V) measurement, also known as the hysteresis measurement, is a widely used method for characterizing a ferroelectric sample. Figure 2.16 illustrates the circuit diagram in a commercial ferroelectric tester (Radiant Multiferroic II) utilized in this thesis for polarization-voltage measurements.

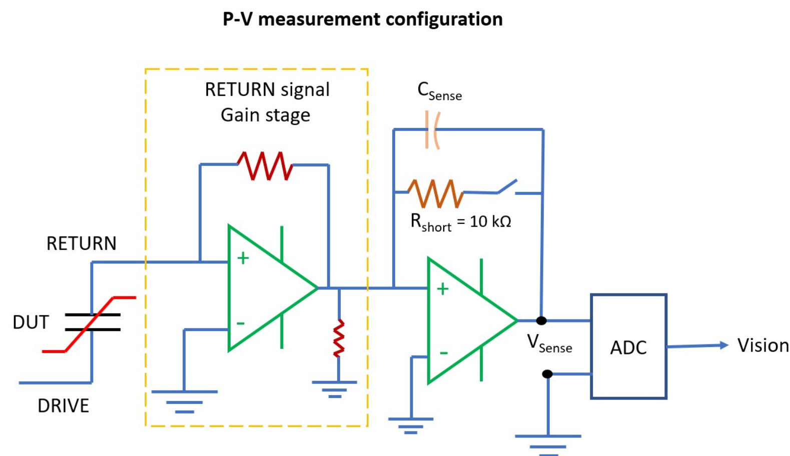

Figure 2.16: Schematic representation of the polarization measurement set-up in the Radiant ferroelectric tester. Figure reconstructed from ref [177].

The tester is controlled by a software called 'Vision'. It allows one to input various measurement parameters and retrieve measured data. The Vision software controls the tester to apply a voltage sweep across the device under test (DUT). As the DUT capacitor charges, a voltage develops at the positive node of the Gain stage amplifier. This produces an amplified voltage output which is passed on to a charge integrator. The voltage output of the charge integrator is directly proportional to the charge on the DUT and the amplification of the gain stage. The Analog-to-Digital Converter (ADC) takes the analog voltage signal from the charge integrator and converts it into a digital representation that a computer or other digital system can process. Knowing the area of the ferroelectric device, the software divides the measured charge by device area to obtain polarization.

Technically in this procedure, a voltage waveform is administered to the sample through a sequence of voltage steps. At each voltage step, the induced current in the sample is integrated, and the resulting integral value is recorded and transformed into polarization using the following formula:

$$\mathrm{Polarization}(\mu\mathrm{C/cm^2}) = \frac{\mathrm{Q}}{\mathrm{Area(cm^2)}} = \frac{\mathrm{C_{Sense}}(\mu\mathrm{F}) \times \mathrm{V_{Sense}}}{\mathrm{Area(cm^2)}} \tag{2.10}$$

The voltage waveform used is a standard bipolar triangular waveform (shown in Figure 2.17), defined by specifying the maximum voltage ($\mathrm{V_{max}}$) and the total duration in milliseconds. The initial leg of the waveform is determined by the voltage polarity. The duration of the waveform primarily dictates the number of data points, which may be adjusted based on the voltage. The Vision software automatically calculates the optimal number of points, maximizing feasibility under specified conditions. Starting at 0.0 volts, the waveform incrementally reaches the assigned maximum voltage, transitions to its negative equivalent, and returns to zero volts.

The time between sampling points, the step delay, is calculated by dividing the total duration by the number of points minus one (shown in Figure 2.17). The voltage step, the change in voltage between points, is determined by dividing four times the maximum voltage by the number of points (shown in Figure 2.17). The integrated value is sampled at the end of each step delay, just before the next voltage change occurs.

There is an option to pre-set the sample by applying the waveform without measurement. The benefit of this is that it establishes the sample in a known polarization state.

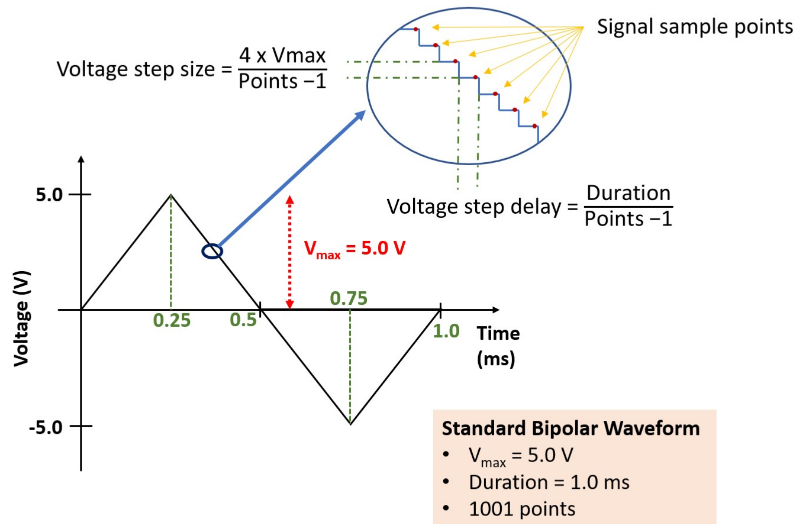

Figure 2.17: Details of the Standard Bipolar drive profile. Figure reconstructed from ref [177].

In the case of the Standard Bipolar waveform, this ensures that both legs of the waveform will influence the sample. The user has the flexibility to program the delay between presetting waveform and measuring waveform. In the present study, this delay was set as 1000 ms. Although this is the standard default operation, a drawback of this option is that signals are applied to the sample without being measured. In the software, an option exists to deactivate the preset pulse before measurement, allowing for an examination of the sample's response to each applied voltage without the influence of preset pulses.

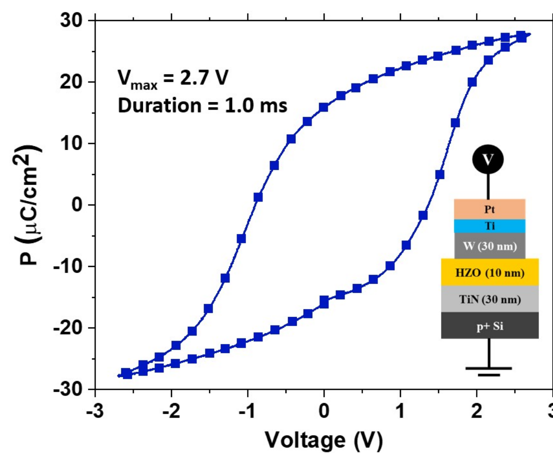

Figure 2.18: P-V measurement on p^{+}Si-TiN-HZO-W stack (shown in inset). V_{max} of 2.7 V and duration of 1.0 ms with a pre-set pulse is used for the measurement.

Figure 2.18 shows the result from P-V measurement performed on a ferroelectric capacitor structure with HZO of 10 nm used as the ferroelectric layer, TiN as the bottom

electrode and W as the top electrode. The measurements are conducted for V_{max} = 2.7 V and duration = 1 ms with a preset pulse.The sample is grounded through the chuck and the voltage is applied on the top electrode. The polarization response of the sample contains ferroelectric displacement, dielectric displacement and static leakage components which includes the tunneling of electrons across the ferroelectric barrier. Although the P-V measurement is useful in understanding the cumulative response of the memory device to the external applied electric field, the remnant polarization value obtained from this measurement is an over-estimation. The Radiant ferroelectric tester tool also has the facility to measure the current directly instead of measuring charge and it is discussed in the following section.

2.5.2 Current-voltage (I-V) measurement

In the current-voltage (I-V) measurement the integrator is set to the ”opened” configuration, as depicted in Figure 2.19. In this setup, the C_{Sense} switch is opened, while the R_{Short} switch is closed, effectively shorting the sample to V_{Sense} through a 10 kΩ resistor. Applying Ohm’s law, the current flowing through the sample can be directly deduced from V_{Sense} by

$$V = I \times R \rightarrow I = \frac{V}{R} = \frac{V_{Sense}}{10000} \tag{2.11}$$

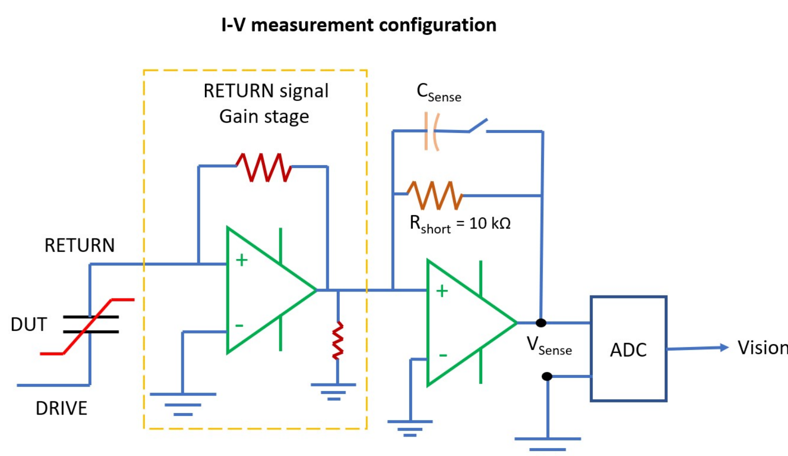

Figure 2.19: Schematic representation of the current measurement set-up in the Radiant ferroelectric tester. Figure reconstructed from ref [177].

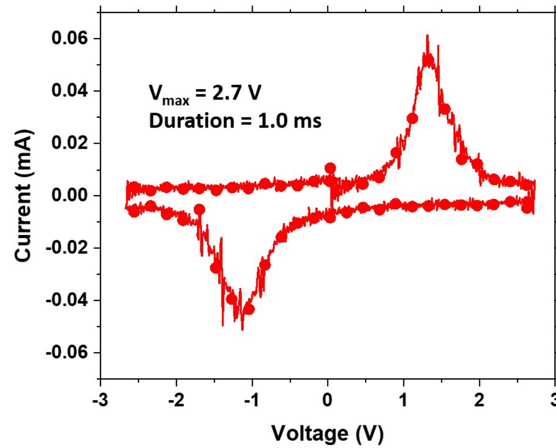

Figure 2.20: I-V measurement on p^+Si-TiN-HZO-W stack.

Different types of waveforms can be used for the I-V measurements. The standard one used for understanding the polarization switching characteristics is the Standard Bipolar waveform shown in Figure 2.17. The I-V measurement performed on the capacitor structure illustrated in the inset of Figure 2.18 is presented in Figure 2.20. The measurement was performed with a Standard Bipolar waveform with a V_{max} value of 2.7 V and duration of 1 ms. The details of the measurement analysis will be discussed in Section 2.6. The coercive voltage distribution and the symmetry of the ferroelectric switching peak can be easily identified from an I-V measurement and this provides valuable insight about the nature of ferroelectric switching in the device under investigation.

2.5.3 PUND P-V measurement

Positive-Up-Negative-Down (PUND) P-V measurement is a technique used to separately measure the polarization from ferroelectric switching (P_{FE}) independent of the dielectric component (P_{DE}) and the static leakage components (P_{Leak}).

A standard PUND measurement consists of a succession of five triangular signals as shown in Figure 2.21. The first pulse of negative polarity marked as 'I', switches the ferroelectric domains to one direction. The second pulse of positive polarity, 'P' short for positive, switches the ferroelectric domains to the opposite direction. The polarization response of this pulse (P_P) contains contribution from the ferroelectric, dielectric and the static leakage components and it can be mathematically represented as:

$$P_P = P_{FE} + P_{DE} + P_{Leak} \tag{2.12}$$

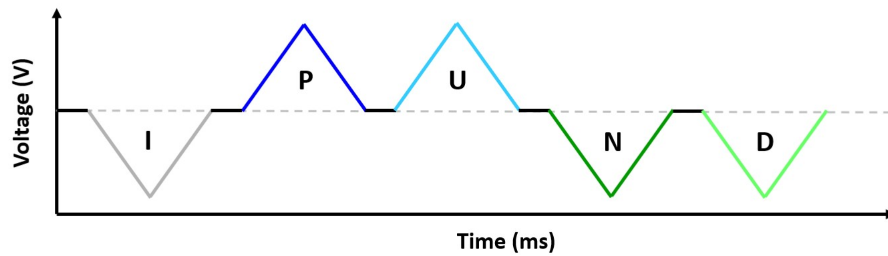

Figure 2.21: Conventional PUND measurement sequence.

The third pulse also has positive polarity and it is marked as 'U' in short for up. As the domains are already switched to the positive direction with the application of 'P' pulse, the polarization response of 'U' pulse only contains the dielectric component and the static leakage component. It can be mathematically represented as:

$$P_U = P_{DE} + P_{Leak} \tag{2.13}$$

The forth pulse has negative polarity and is noted as 'N' in short for negative. This pulse switches the polarization to the opposite direction and thus, the polarization response of this pulse (P_N) can be represented as:

$$P_N = P_{FE} + P_{DE} + P_{Leak} \tag{2.14}$$

Finally, the fifth pulse also has negative polarity. This pulse is marked as 'D' in short for down. As the polarization was already switched to this direction with the application of 'N' pulse, the response to this pulse only have the dielectric and static leakage components.

$$P_D = P_{DE} + P_{Leak} \tag{2.15}$$

By calculating P_P - P_U and P_N - P_D, we can separate the P_{FE} component corresponding to the positive and negative polarities of the applied voltage pulse respectively.

The Radiant ferroelectric tester employs a modified approach for PUND P-V measurement, maintaining the above mentioned fundamental principle while deviating in execu-

tion. Instead of utilizing the pulse sequence illustrated in Figure 2.21, it adopts a distinct measurement sequence depicted in Figure 2.22. The PUND P-V measurement, focused solely on the remnant component, is derived through a combination of two hysteresis loops known as Logic 1 and Logic 0.

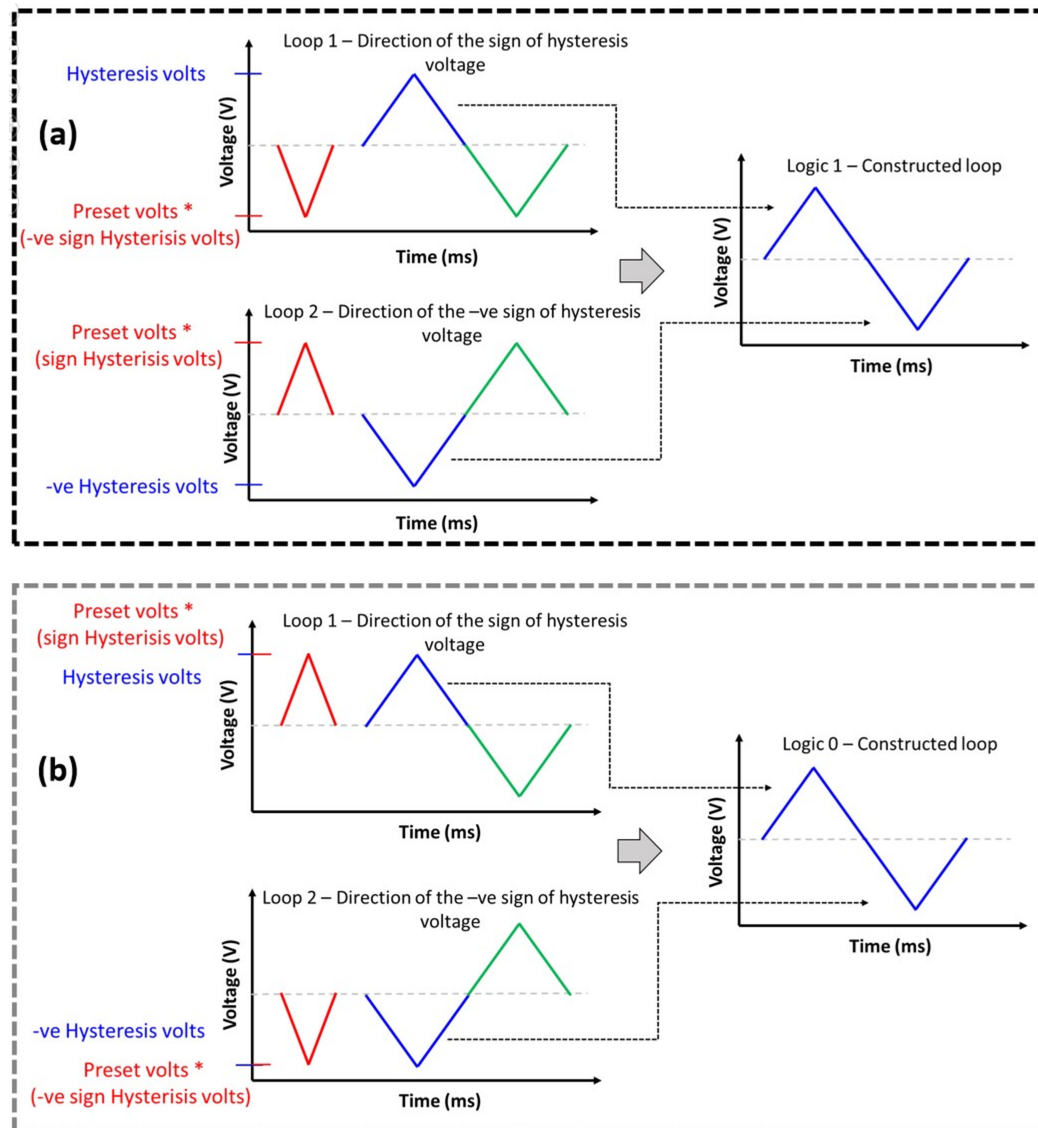

Figure 2.22: Schematic representation of the PUND measurement sequence in the Radiant ferroelectric tester: (a) The construction of the Logic 1 loop containing both remnant and non-remnant components. (b) The construction of the Logic 0 loop containing only the non-remnant component. Figure reconstructed from ref [177].

The Logic 1 loop represents a hysteresis measurement where both legs of the applied Standard Bipolar waveform induce polarization switching, shown in Figure 2.22(a). Consequently, this measurement contains both remnant and non-remnant components. In contrast, the Logic 0 loop embodies a hysteresis measurement where neither leg trig-

gers polarization switching, containing only non-remnant polarization, shown in Figure 2.22(b). Subtracting the Logic 0 loop from the Logic 1 loop results in the remnant-only loop.

Both the Logic 1 and Logic 0 loops are synthesized combinations of two actual measurements. The Logic 1 loop is constructed by preceding a standard hysteresis measurement with a preset pulse that sets the sample to a polarization opposite to the direction of the first leg of the pulse. This ensures the first leg switches the sample, and the first half of the sample polarization response is saved as the initial part of the Logic 1 response. The polarity of both the preset pulse and the hysteresis loop is then reversed, and the measurement is repeated to capture the sample switching to the opposite polarization state. In this case, the first half of the sample response is saved as the second half of the Logic 1 response.

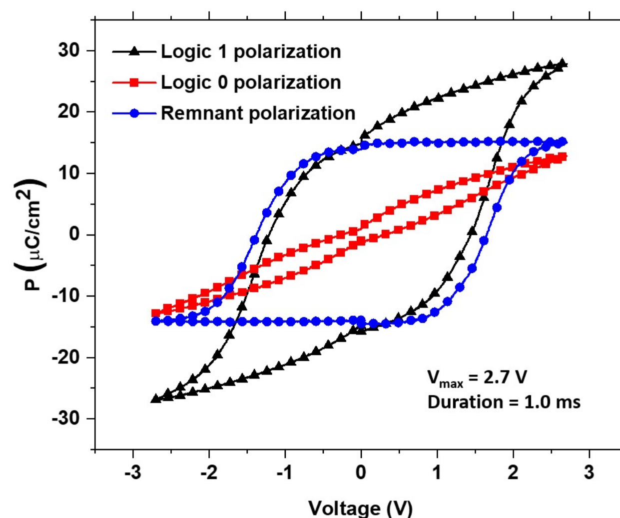

Figure 2.23: PUND P-V measurement on p^+Si-TiN-HZO-W stack.

In the measurement set-up, the parameters which the user has control over are the maximum hysteresis voltage (V_{max}), duration of the measurement pulse, maximum voltage of the preset pulse, preset pulse duration and a delay between preset pulse and the measurement pulse. As a standard procedure, we always use the same V_{max} for the measurement pulse and the preset pulse. The delay between preset pulse and the measurement pulse is kept as 1000 ms. Also, the duration of the preset pulse and the measurement pulse are always kept equal.

The PUND P-V measurement conducted on the capacitor structure illustrated in the

inset of Figure 2.18 is presented in Figure 2.23. The measurement was performed with a V_{max} of 2.7 V and pulse duration of 1 ms. The polarization measurement corresponding to the Logic 1, Logic 0 and the remnant polarization (Logic 1 - Logic 0) is shown in Figure 2.23.

2.5.4 Small signal capacitance-voltage (C-V) measurement

Ferroelectrics demonstrate a nonlinear response in capacitance-voltage (C-V) characteristics. The capacitance measurement technique involves applying a small AC signal atop a DC bias. Utilizing a Keysight B1500A semiconductor parameter analyzer tool, the capacitance is determined at a fixed AC amplitude and frequency for each DC voltage step. On approaching the coercive voltage, the material showcases a notable increase in permittivity, resulting in a corresponding surge in capacitance. This occurrence repeats twice in a ferroelectric material, generating a distinctive butterfly-like loop in the C-V curve. The selection of the AC signal frequency depends on the specific application, commonly ranging from 1 kHz to 1000 kHz. When the thickness of the ferroelectric material is known, this method becomes instrumental in extracting critical information such as coercive voltage (V_c) and relative permittivity (ϵ_r). These parameters offer insights into the predominant crystal phase and may reveal the presence of space charge effects, contributing to a comprehensive understanding of the behavior of ferroelectric material.

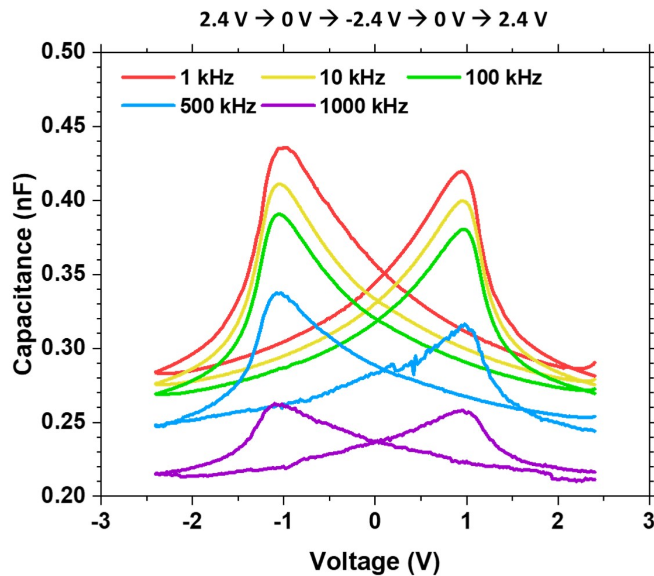

Figure 2.24: C-V measurement at different AC frequencies (1-1000 kHz) on p^+Si-W(30 nm)-HZO (10 nm)-W(100 nm) stack.

C-V measurement performed at different AC frequencies (1 kHz - 1000 kHz), on a p^+Si-W-HZO-W device with 95 $\times$ 95 μm^2 area is shown in Figure 2.24. In this setup, the voltage is swept from 2.4 V to 0 V, then to -2.4 V, back to 0 V, and finally to 2.4 V. The quasi-static voltage increment is set at 25 mV, while an AC signal with a voltage amplitude of 20 mV is applied on top of the DC bias. In this context, the measured capacitance directly correlates with the permittivity of the HZO material. As the frequency of the AC signal rises, the measured capacitance diminishes, signaling a decrease in permittivity. The permittivity is influenced by the oscillation of free dipoles in response to an alternating electric field. With increasing frequency, these dipoles start to lag behind the changes in the electric field, resulting in a reduction in permittivity [178, 179].

2.5.5 Reset-read-set-read measurements

The measurement sequence used for measuring the OFF and ON state current in a FTJ memory device is called the 'Reset-read-set-read' measurement. 'Reset' operation is used to switch the polarization in the device to the high resistance state, called the OFF state. Whereas the 'Set' operation is used to switch the polarization to the opposite direction which leads to the low resistance state, called the ON state of the memory device. The reset and set operations are performed with the Radiant ferroelectric tester tool by performing a current loop measurement with monopolar pulse of desired shape, amplitude and duration. To prevent the application of additional voltage pulses, the preset option of the current loop measurement is deactivated during the Reset or Set operation. The 'Read' operation involves measuring the leakage current following the Reset or Set operation. This measurement aims to assess the resistance state of the memory device following the preceding Reset or Set operation. The Read voltages must be carefully selected to ensure that they do not affect the polarization state of the device, enabling non-destructive measurement. The Reset and Set pulses have opposite polarities. The read measurement is performed with the same voltage pulse for measuring both the OFF and ON state currents. As a convention, the polarity of the chosen Read voltage aligns with the polarity of the Set pulse.

Throughout this study, we performed the Read operation in two different ways. In one method, a quasi-static voltage pulse is applied and corresponding current is measured at

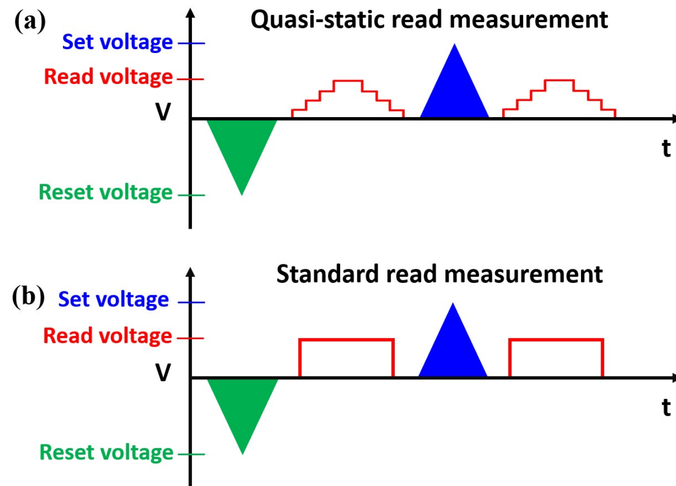

Figure 2.25: Measurement sequence corresponding to (a) Quasi-static read measurement and (b) Standard read measurement.

each voltage steps. These measured current values are then plotted across the corresponding voltage value. This measurement is known as the 'Quasi-static read' measurement, shown in Figure 2.25(a). To conduct the quasi-static read measurement, we utilized the B1500A tool. In the second method, Read current measurement in the memory device is performed by applying a DC voltage pulse and measuring the corresponding current. For attaining a single value corresponding to the OFF and ON state, we average the current measured across the duration of the DC voltage pulse. This type of measurement is known as the 'Standard read' measurement, shown in Figure 2.25(b). The standard read measurement was performed with the help of Radiant ferroelectric tester.

2.5.6 Partial switching measurements for multiple resitance states

In M-FE-DE-M FTJ devices, the polarization of the ferroelectric layer influences the tunneling current across the tunneling barrier at a given read voltage. By adjusting the polarization of the ferroelectric layer, it is possible to achieve different resistance states for the same read voltage. The increase in conductivity of the FTJ devices, achieved by switching more domains to the Set polarization, is known as 'potentiation.' Conversely, the decrease in conductivity, achieved by switching more domains to the Reset polarization, is known as 'depression.' To demonstrate multiple resistance states, it is essential to switch the domains in the ferroelectric layer gradually or partially. This technique, known as partial switching of domains, is achieved by using Reset or Set voltage pulses with re-

duced amplitude or pulse width, ensuring that not all domains switch simultaneously.

Partial switching can be accomplished in three different ways. One effective method involves voltage modification of the Reset/Set pulses, shown in Figure 2.26(a). This process begins with a full Reset operation, where all domains are switched to the Reset polarization. Following this, a small Set voltage, significantly lower than the coercive voltage, is applied to the device, and the corresponding ON current is measured using a DC read (standard read) measurement. The Set pulse amplitude is then slightly increased, and another DC read measurement is taken. This cycle is repeated, incrementally increasing the Set pulse amplitude and performing DC read measurements until full polarization switching is achieved. After completing the Set pulse sequence, a small Reset voltage is applied, and a DC read measurement is taken. The Reset pulse amplitude is then gradually increased, with corresponding DC read measurements taken after each increment, until a full Reset operation and final read measurement are performed. This systematic approach ensures precise control over the partial switching of domains, facilitating the demonstration of multiple resistance states.

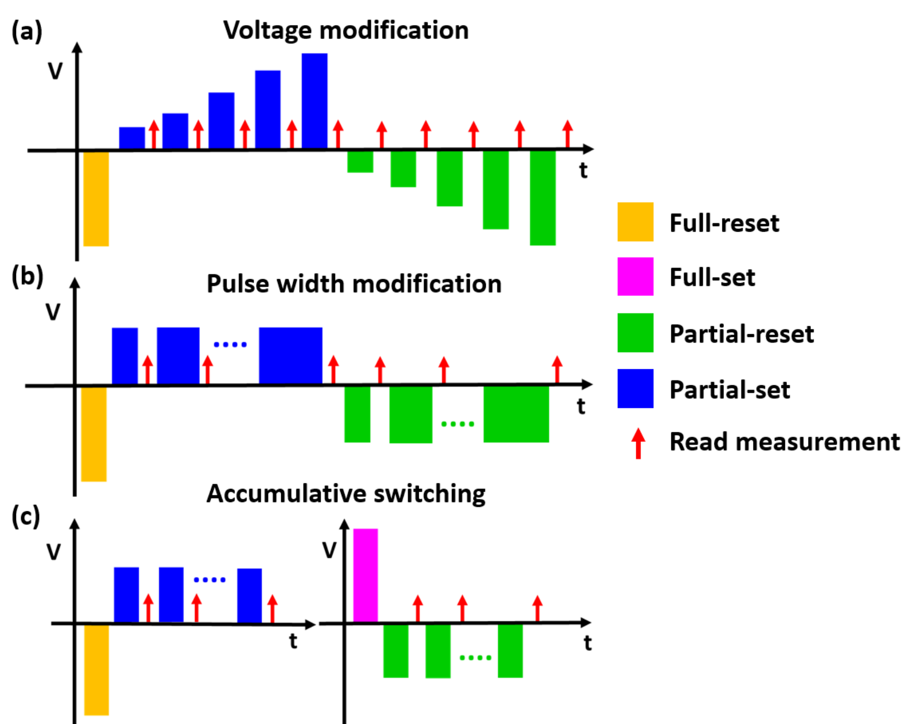

Figure 2.26: Schematic representation of the pulse sequences used to achieve multiple resistance states through partial switching operations: (a) voltage amplitude modification, (b) pulse width modification, and (c) accumulative switching of the Reset and Set voltage pulses.

The second method involves modifying the pulse width of the Reset and Set pulses, shown in Figure 2.26(b). In this approach, the voltage amplitude of the Reset and Set pulses is fixed, and the pulse width is gradually increased to achieve partial switching of domains. The voltage amplitudes for these pulses are determined based on the results from the voltage amplitude modification measurements, specifically selecting the voltage at which polarization switching begins to occur. The pulse width is typically varied from 0.5 ms to 1000 ms. After each Reset/Set pulse, a DC read measurement is performed to measure the read current of the FTJ device.

The third method involves applying the same partial switching Reset or Set pulses multiple times to achieve partial switching of domains, a process known as accumulative switching. This is shown in Figure 2.26(c). In this approach, the voltage amplitude and pulse width of the Reset and Set pulses are fixed. By repeatedly applying the same pulse, domains are incrementally switched one by one. This method is the most challenging type of partial switching process to demonstrate. After each partial switching Reset/Set operation, a DC read measurement is performed to assess the read current of the FTJ device.

In this thesis, the partial switching Reset, Set, and DC read measurements were conducted using the Radiant ferroelectric tester tool. Custom programs were developed using the tool's Vision software to apply the voltage and measurement pulses sequentially. The parameters that can be controlled include the pulse shape, amplitude, and pulse width of the Reset and Set pulses, as well as the read voltage amplitude and read time. However, due to software limitations, the time interval between pulses cannot be controlled.

2.6 Electrical characterization of M-FE-M stacks

In this section, we study the electrical characterization of four distinct metal-ferroelectric-metal (M-FE-M) stacks depicted in the Figure 2.27. These stacks exhibit variations in their bottom and top electrodes. Stack M1 consists of a 30 nm TiN bottom electrode and a 100 nm TiN top electrode. Stack M2 features a 30 nm TiN bottom electrode and a 100 nm W top electrode. Stack M3 comprises a 30 nm W bottom electrode and a 100 nm TiN top electrode. Lastly, stack M4 is comprised of a 30 nm W bottom electrode and a 100 nm W top electrode. The fabrication process for these four MFM stacks follows the

procedure outlined in section 2.4.1, where the bottom electrode is blanket deposited and the top electrode is patterned via a lift-off process. The stacks undergo RTP annealing at 400 °C for 180 seconds in an N_2 atmosphere. Here, Dr. Wassim Hamouda performed the ALD deposition of the HZO layer and the RTP annealing during the stack fabrication.

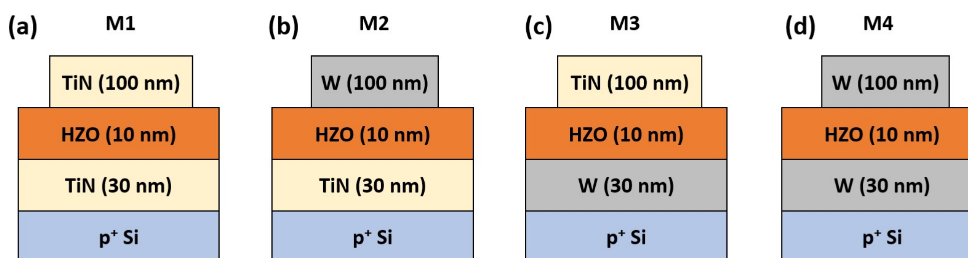

Figure 2.27: M-FE-M stacks with varying combinations of top and bottom electrodes. (a) Stack M1: TiN for both top and bottom electrodes. (b) Stack M2: TiN bottom electrode and W top electrode. (c) Stack M3: W bottom electrode and TiN top electrode. (d) Stack M4: W for both bottom and top electrodes.

The switching I-V measurement performed on these 4 stacks at pristine, after 2000 and 10^5 cycles are shown in Figure 2.28(a), (b) and (c), respectively. Wake-up cycling is performed using a triangular pulse with a frequency of 1 kHz and an amplitude of 2.4 V for stacks M1, M3, and M4, while stack M2 employs a 2.3 V amplitude. For I-V measurements, a triangular pulse with a 1 ms pulse width and an amplitude of 2.4 V is used for stacks M1, M3, and M4, and 2.3 V for stack M2. In the pristine state, M1 and M2 stacks show two well seperated peaks in the positive and negative polarity, as shown in Figure 2.28(a). This type of coercive voltage distribution indicates antiferroelectric like switching behaviour [180, 181]. The same phenomenon is observed in the P-V measurement, with identical parameters to those of the I-V measurement, as depicted in Figure 2.28(d). For stack M3 and M4, the two peaks are not well-separated and appear moderately merged together, resulting in a broad coercive voltage distribution. The P-V measurement for M3 and M4 stacks exhibit ferroelectric-like behavior from the pristine state onwards. The PUND P-V measurement performed on these 4 stacks at pristine state is shown in Figure 2.28(g). Stack M1 shows the lowest remnant polarization value of 6.4 μC/cm^2 in the pristine state. Stacks M2, M3 and M4 shows remnant polarization value of 9.0 μC/cm^2, 17.3 μC/cm^2 and 18.1 μC/cm^2 respectively.

After 2000 cycles, the I-V measurements reveal a merging of the distinct switching peaks observed in the pristine state within stacks M1 and M2. This results in a broad dis-

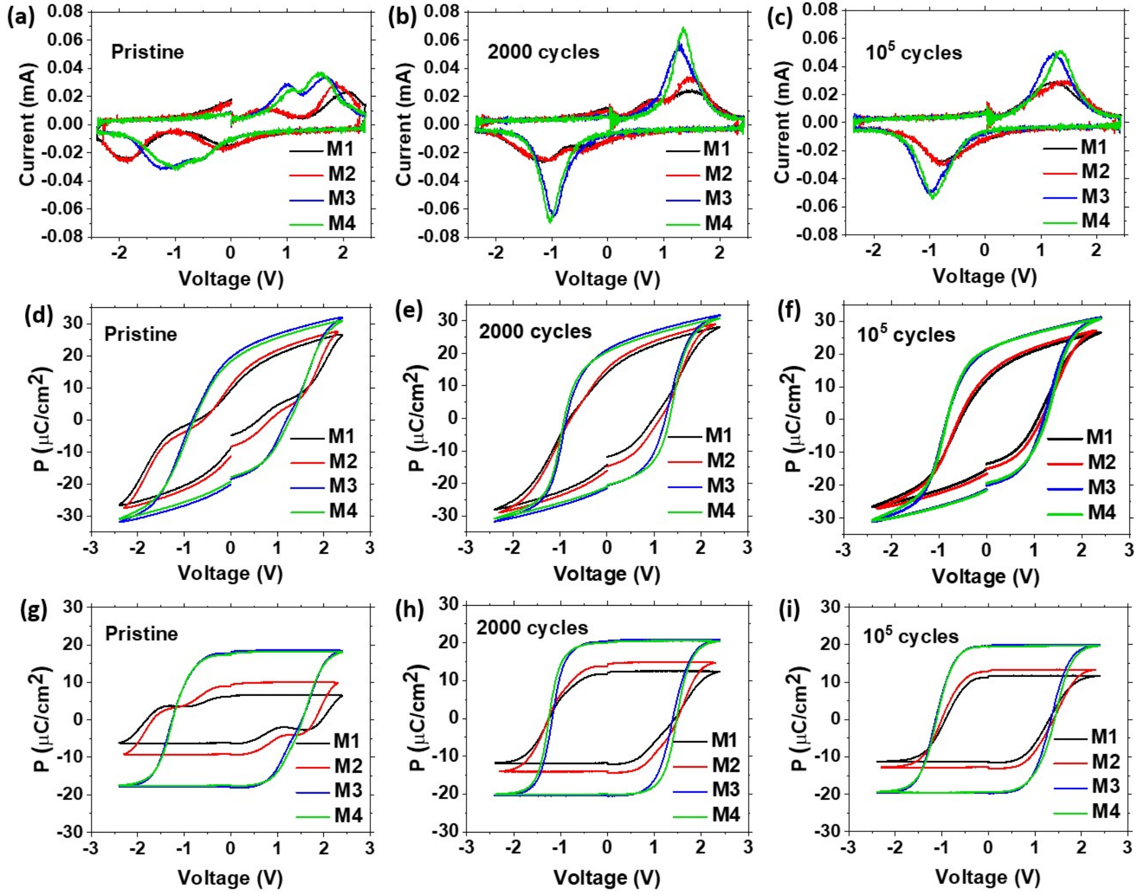

Figure 2.28: Electrical characterization of the four M-FE-M stacks shown in Figure 2.27. (a-c) I-V measurements, (d-f) P-V measurements and (g-i) PUND P-V measurements for pristine, after 2000 and 10^5 cycles.

tribution of coercive voltages (see Figure 2.28(b)). This merging suggests the occurrence of wake-up effects [180]. Such phenomena are also evident in the P-V measurements depicted in Figure 2.28(e), as well as in the PUND P-V measurements shown in Figure 2.28(h), following 2000 cycles. The switching I-V peak corresponding to the stacks M3 and M4 after 2000 cycles have a sharp peak with narrow coercive voltage distribution. The switching I-V peak from stack M3 and M4 indicates a clear wake-up, where the domains are switching within a short voltage range. The P-V loop of stacks M1 and M2 no longer exhibits the characteristic antiferroelectric profile after 2000 cycles. However, it has not fully transitioned into a ferroelectric-like state either. Rather, it appears to reside in an intermediate phase of the transition. Based on the PUND P-V measurement after 2000 cycles, depicted in Figure 2.28(h), it is observed that stacks M1, M2, M3, and M4 exhibit remnant polarization values of 12.1 $\mu C/cm^2$, 14.3 $\mu C/cm^2$, 20.1 $\mu C/cm^2$, and 20.6 $\mu C/cm^2$, respectively.

After 10^5 cycles, the switching I-V curves from all four stacks exhibit characteristics resembling ferroelectric switching behavior, as illustrated in Figure 2.28(c). This is also visible in the P-V measurement as shown in Figure 2.28(f). The PUND P-V measurements after 10^5 cycles, as depicted in Figure 2.28(h), yield remnant polarization values of 11.6 μC/cm^2, 13.2 μC/cm^2, 19.4 μC/cm^2, and 19.8 μC/cm^2 for stacks M1, M2, M3, and M4, respectively. Comparing the PUND P-V measurements at pristine, 2000, and 10^5 cycles reveals an initial increase in remnant polarization from pristine to 2000 cycles, suggesting a wake-up effect. However, the polarization subsequently decreases with cycling to 10^5 cycles, indicating fatigue.

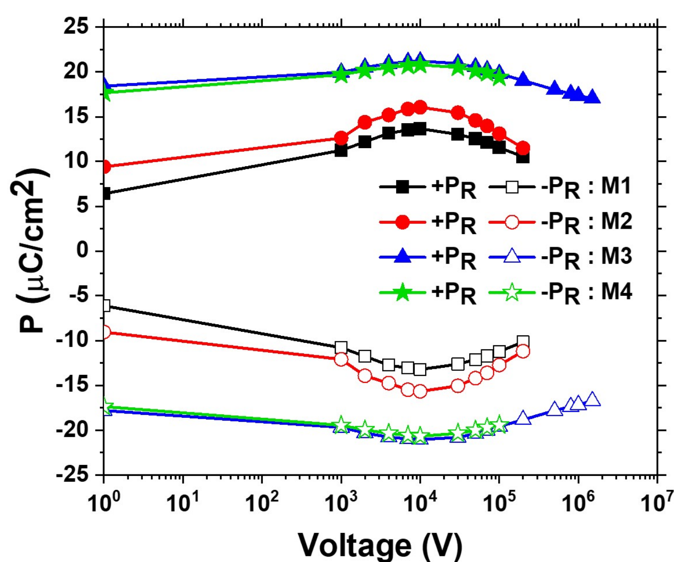

Figure 2.29: The evolution of remnant polarization from the pristine state to 'n' cycles, where 'n' represents the endurance of the device, is illustrated for various M-FE-M stacks, as depicted in Figure 2.27.

Figure 2.29 illustrates the evolution of remnant polarization (P_R) from the pristine state to 'n' cycles, where 'n' represents the endurance of the device. All four stacks demonstrate an endurance exceeding 10^5 cycles. Among all stacks, Stack M1 exhibits the lowest P_R. Stack M3 and M4 demonstrate similar trends in the evolution of P_R, displaying the highest P_R values among the four stacks. This comparison reveals that M1 and M2 stacks exhibit similar polarization switching behavior, while M3 and M4 stacks also demonstrate similarity in their behavior. Notably, M1 and M2 stacks share TiN as the bottom electrode, with differing top electrodes, whereas M3 and M4 stacks feature W as the bottom electrode, also with differing top electrodes. The consistent behavior observed

in stacks with similar bottom electrodes suggests that the bottom electrode may exert a significant influence on the polarization of the ferroelectric layer. These results serves as a reference point for the fabrication and understanding of the more complex FTJ device stacks with M-FE-DE-M architecture, which will be discussed in the following chapters.

Chapter 3

Bilayer FTJ Investigation

3.1 Introduction

In this chapter, we undertake a thorough examination of the diverse elements influencing the optimization of FTJ bilayer stack architecture. As the physical dimensions of FTJ devices reach the nanoscale, new challenges arise that demand innovative strategies to maximize their efficiency and reliability. The arrangement of constituent materials, layer thicknesses, and interfaces can profoundly influence the device's properties, such as polarization stability, switching characteristics, and overall functionality. Understanding and mitigating issues related to interfacial engineering, material selection, and strain management are crucial steps in attaining desired outcomes. Moreover, the selection of suitable deposition techniques, growth conditions, and fabrication processes adds further complexity. Within the context of this chapter, we aim to shed light on the fundamental principles that govern FTJ bilayer stack behavior and explore the interplay between materials and architecture for attaining the most favorable device performance.

In FTJ bilayer stack with M-FE-DE-M architecture, the tunneling across the DE layer is controlled by the polarization of the FE layer as explained in Chapter 1. Despite recent studies and demonstrations of FTJ functionalities using these stacks [121, 140], there is a need to investigate how the positioning of metal electrodes, dielectric, and ferroelectric layers affects the interfaces, and subsequently, how this impacts FTJ performance. The ferroelectricity in hafnium oxide depends on various parameters like doping, crystallization conditions, capping metals, etc [182]. A recent study has shown that in case of

ferroelectric HZO layer, using TiN bottom electrode and W top electrode leads to higher remnant polarization in M-FE-M stack than TiN bottom electrode and Au, Pt, TiN and Ta top electrodes [183]. We also observe this phenomenon in our own M-FE-M stacks as discussed in Section 2.6. The stack featuring a TiN bottom electrode and W top electrode exhibits a higher remnant polarization compared to the stack with TiN serving as both the bottom and top electrode. The remnant polarization is even higher for stacks with W bottom electrode and TiN or W top electrodes. As the coefficient of thermal expansion of the top electrode decreases, the in-plane strain changes from compressive to tensile strain and leads to an increase of the ferroelectric orthorhombic phase crystallization [73]. In contrast to the M-FE-M stack, the bilayer FTJ features two metal electrodes that interfaces with different oxides (HZO and the tunneling oxide), experiencing distinct process conditions. The interface between the top electrode and oxide undergoes crystallization annealing only, whereas the bottom interface is also subjected to the oxides deposition process above it. Hence, the interfaces may also exert a significant influence on the device's operation. TiN acts as the diffusion barrier layer in CMOS back-end, and W is commonly used for Vias. This facilitates the seamless integration of FTJ devices with these metal electrodes, necessitating minimal adjustments to the back-end-of-line (BEOL) process. Despite the clear advantages of these metals, the positioning of the metals may significantly impact the FTJ performance. Therefore, optimizing the stack architecture is essential to achieve high performance.

For the fabrication of bilayer stacks we use W and TiN electrodes, HZO ferroelectric layer and $\mathrm{Al_2O_3}$ dielectric layer. The W and TiN electrodes are deposited by sputtering at room temperature and their thickness is targeted to be 30 nm. The HZO layer is deposited by ALD, as discussed in Section 2.1.2. The $\mathrm{Al_2O_3}$ layer is deposited by ALD at 250 °C using TMA precursor. To achieve the ferroelectric orthorhombic phase in the HZO layer, the entire stack undergoes annealing via RTP at 400 °C for 120 seconds in an N_2 ambient following the deposition of the top metal. Marco Holzer, Dr. Sourish Banerjee and Dr. M. H. Raza performed the deposition of the HZO and $\mathrm{Al_2O_3}$ layers for the devices, as well as the RTP annealing of the stacks discussed in this chapter. Subsequently, square pads with dimensions of 95 $\times$ 95 $\mu\mathrm{m}^2$ are patterned in the top electrode layer using the process flow outlined in Section 2.4.2.

In this chapter, we begin by investigating the influence of dielectric positioning on the FTJ device with a TiN bottom electrode and W top electrode. Then, we explore the impact of metal positioning by swapping the positions of the metals while maintaining the dielectric near the top electrode. We also examine how variations in dielectric thickness impact FTJ performance. Additionally, we analyze whether different fabrication process flows for the same FTJ stack architecture affect its performance. This chapter provides insights into the role of charge traps in facilitating robust polarization, particularly when the ferroelectric layer is in contact with a dielectric on one side.

3.2 Effect of dielectric positioning

For the bilayer FTJ stack, the dielectric can be placed either near the bottom electrode or near the top electrode. As the bottom electrode experiences different processing conditions depending on what layer is deposited on top of it, its interface can vary from one stack to the other. As the FTJ works on the principle of tunneling, the interface plays a crucial role in the tunneling barrier offset as well as on the stabilization of polarizing by charge screening [128, 184, 185]. To understand the impact of dielectric location on FTJ devices with TiN bottom electrode and W top electrode, two stacks as shown in Figure 3.1(a) and (d) are fabricated on p+ Si substrate. A TEM image of the device cross-section of stack A and stack B is shown in Figure 3.2(a) and (b) respectively.

For both the stacks, the thickness of the HZO layer is 10 nm and that of the $\mathrm{Al_2O_3}$ layer is 3 nm. In the case of stack A, the dielectric $\mathrm{Al_2O_3}$ is placed near the top W electrode and in the case of stack B, the dielectric $\mathrm{Al_2O_3}$ is placed near the bottom TiN electrode. The switching I-V measurements corresponding to stacks A and B are shown in Figure 3.1(b) and Figure 3.1(e) respectively. The PUND sequence P-V measurements corresponding to the stacks A and B are shown in Figure 3.1(c) and Figure 3.1(f) respectively. Even though the thickness of ferroelectric, dielectric, and metal layers are identical for the two stacks, the switching voltages are different. The maximum voltage for which the device does not break down during the switching operation and cycling operation is chosen as the device operating voltage. For stacks A and B, the operating voltages ($|\mathrm{V_{max}}|$) are 4.0 V and 5.0 V respectively. The wake-up cycling operation is carried out with a bipolar triangular pulse of 100 Hz frequency and $\mathrm{V_{max}}$ amplitude. The voltage is

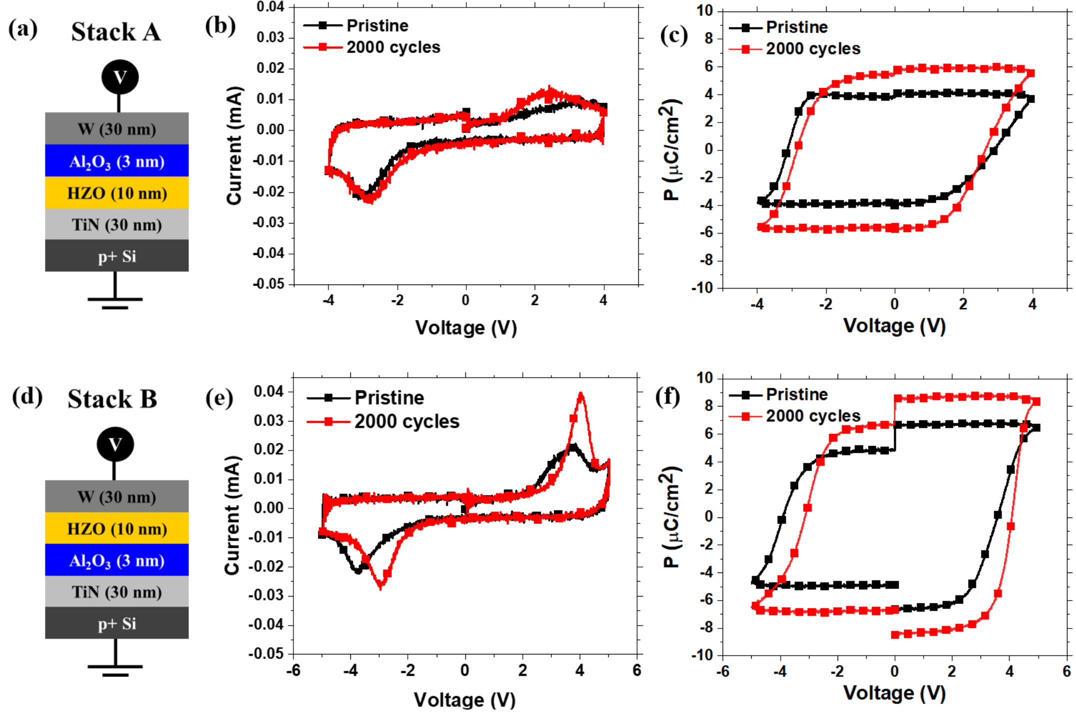

Figure 3.1: (a) Schematic of stack A, the p+Si (substrate)-TiN-HZO-Al_2O_3-W FTJ device. (b) The switching I-V curves corresponding to stack A at pristine state and after wake up of 2000 cycles. (c) The PUND sequence P-V measurement corresponding to stack A at pristine state and after 2000 cycles. (d) Schematic of stack B, the p+Si (substrate)-TiN-Al_2O_3-HZO-W FTJ device. (e) The switching I-V curves corresponding to stack B at pristine state and after 2000 cycles. (f) The PUND sequence P-V measurement corresponding to stack B at pristine state and after 2000 cycles. For both the stacks, the wake-up cycling is performed with triangular pulses of 100 Hz frequency. The voltage amplitude used for wake-up cycling are $\pm$ 4.0 V, $\pm$ 5.0 V for stacks A and B respectively. The switching I-V and P-V measurements are performed with triangular pulses of $\pm$ 4.0 V, $\pm$ 5.0 V amplitudes for stack A and B respectively and 1 ms pulse width.

applied through the patterned top electrode and the substrate is grounded.

For stack A, the switching I-V curve shows a large coercive voltage distribution and the PUND measurement shows a P_R value of $\sim 4.0\mu C/cm^2$ in the pristine state. Whereas in case of stack B, the switching I-V curve shows a large coercive voltage distribution and exhibits a discontinuity between the positive and negative polarities of the PUND P-V measurement. The negative polarity shows smaller P_R value compared to the positive polarity. In the negative polarity, the remnant polarization value is $\sim 4.9\mu C/cm^2$ and in the positive polarity it is $\sim 6.7\mu C/cm^2$. This discontinuity is not observed in stack A. The discontinuity in the PUND P-V measurement can be due to domain switching asymmetry or the different HZO interface in the top and bottom part. Like in the case

of M-FE-M capacitor stacks, these M-FE-DE-M FTJ stacks also show wake-up behavior. After the wake-up of 2000 cycles, stack A still has a large coercive voltage distribution and $\mathrm{P_R}$ value is slightly increased to $\sim$ 6 $\mu\mathrm{C/cm^2}$. For stack B, the coercive voltage distribution narrows compared to the pristine state for both polarities following wake-up. Additionally, the coercive voltage peak for negative polarity shifts to a lower magnitude in stack B from pristine to 2000 cycles. Here, the $\mathrm{P_R}$ increases from $\sim$ 4.9 $\mu\mathrm{C/cm^2}$ to $\sim$6.7 $\mu\mathrm{C/cm^2}$ for negative polarity and the $\mathrm{P_R}$ increases from $\sim$ 6.7 $\mu\mathrm{C/cm^2}$ to $\sim$ 8.6 $\mu\mathrm{C/cm^2}$ for positive polarity. The $\mathrm{P_R}$ values from these stacks after wake-up is much lower than those observed in M-FE-M stacks discussed in Section 2.6. This is because the dielectric layer can only partially compensate the polarization charges at the HZO-$\mathrm{Al_2O_3}$ interface. From the PUND P-V measurements, it is evident that stack B shows a higher polarization compared to stack A.

The evolution of ON and OFF state currents from pristine to 10^4 cycles for stack A and B are shown in Figure 3.3(a). For stack A, reset voltage ($\mathrm{V_{Reset}}$) of +4.0 V and set voltage ($\mathrm{V_{Set}}$) of -4.0 V are used to switch the polarization to the high (OFF state) and low (ON state) resistance states. For stack A, the DC read voltage is -1.4 V. For stack B the reset, set and read voltages are -5.0 V, +5.0 V and +2.0 V, respectively. From Figure 3.3(b) we can see that stack A is having the lowest ON/OFF ratio of $\sim$2 and stack B has a better ON/OFF ratio of $\sim$4. This trend is consistent with the $\mathrm{P_R}$ measurement shown in Figure 3.1. Higher $\mathrm{P_R}$ directly correlates to high ON/OFF ratio and this is consistent with the results by Max et al [119]. One of the advantages of FTJ memory device is that by gradually switching the polarization from one state to the other, it is possible to attain multiple resistance states. But in order to attain multiple well separated resistance states, the FTJ device should have a high ON/OFF ratio as well as high ON-OFF current value. The difference between ON and OFF currents (ON-OFF current) from pristine to 10^4 cycles is shown in Figure 3.3(c). The quasi-static I-V read measurement corresponding to stack A and stack B after 2000 cycles of wake-up are shown in Figure 3.3(d). For stack A, the voltage is quasi-statically swept until -1.4 V on the patterned top electrode. For stack B, the voltage is swept until +2.0 V. Here we can clearly see that there is a higher separation between ON state and OFF state for stack B. Stack B shows higher ON/OFF ratio as well as a higher ON-OFF current value, which makes this stack more suitable

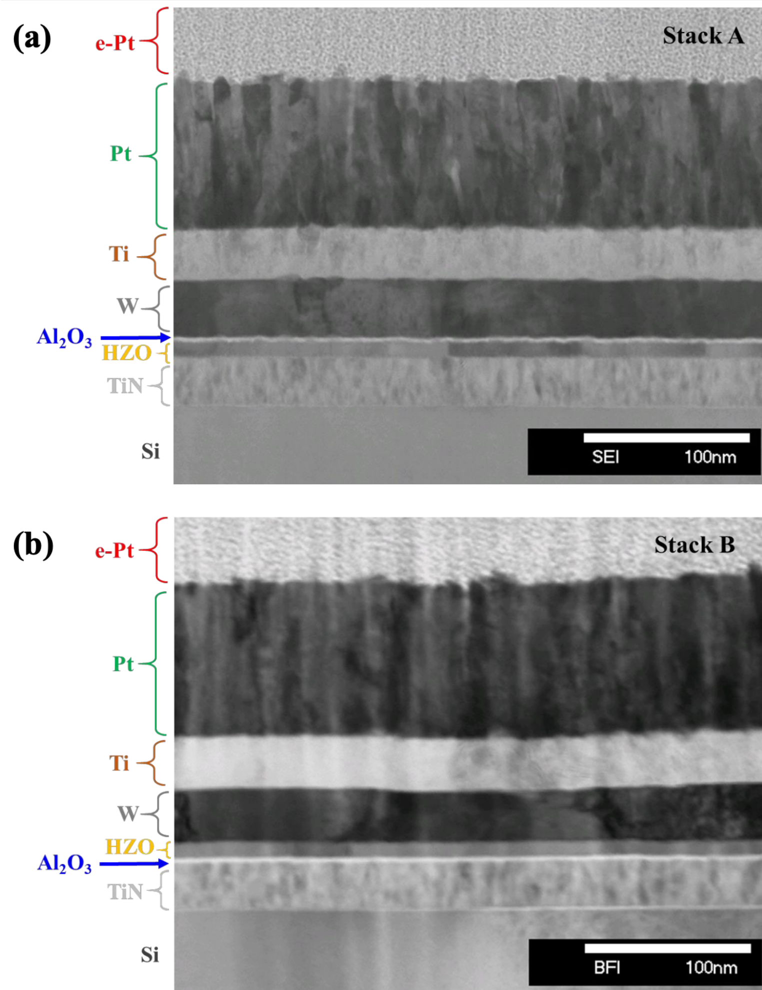

Figure 3.2: (a) TEM image of the device cross section of stack A (b) TEM image of the device cross section of stack B. The TEM images were taken by Dr. I. Häusler (group of Prof. C. T. Koch) of Institut für Physik, Humboldt-Universität zu Berlin.

than stack A.

For both stacks A and B, TiN metal is used as the bottom electrode. It is known that TiN metal tends to oxidize more than the W metal, due to relatively lower negative standard heat of formation of TiO_X (from -105.6 to -154.9 kcal/mol) compared to that of WO_X (-201.4 kcal/mol for WO_3 and -140.9 kcal/mol for WO_2) [186]. So, it is likely that there is a thin TiO_X layer of unknown thickness at the HZO/TiN interface in stack A and Al_2O_3/TiN interface in stack B. The presence of TiO_2 and TiO_X on stack A bottom electrode interface is confirmed with HAXPES measurement (shown in Figure 3.7(a)). Thus, the differences in device performance between stack A and stack B can be understood from the band diagram by including an additional TiO_X layer near the bottom electrode in the bilayer stack. The modified band diagram at OFF state and ON state corresponding

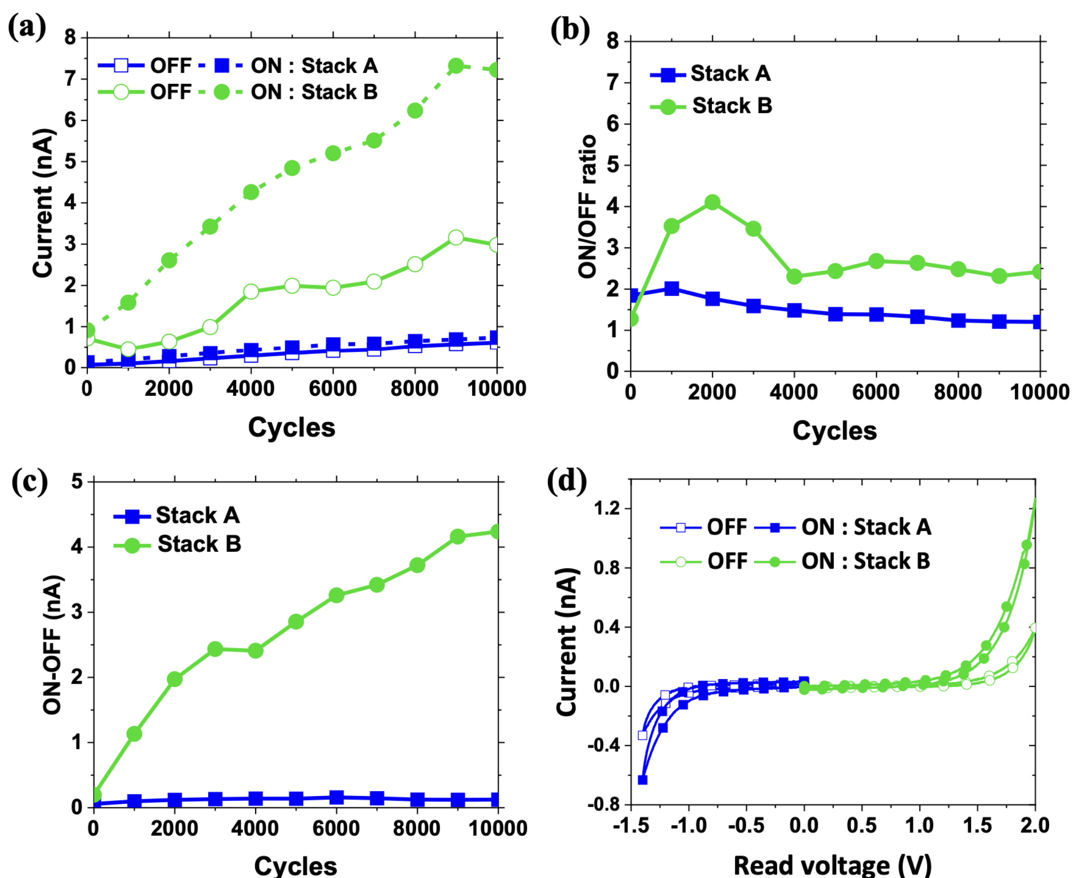

Figure 3.3: (a) Evolution of ON and OFF currents from pristine state to 10^4 cycles for stacks A and B. (b) Evolution of ON/OFF ratio, from pristine state to 10^4 cycles for stacks A and B (c) Evolution of ON and OFF current difference, from pristine state to 10^4 cycles for stacks A and B. (d) Quasi-static read measurement corresponding to stacks A and B after wake-up of 2000 cycles. This read I-V operation is a DC measurement where the voltage is swept quasi-statically. Set and reset operations use a 0.5 ms monopolar triangular pulse. For stack A, the reset, set, and read voltages are +4.0 V, -4.0 V, and -1.4 V, respectively. For stack B, they are -5.0 V, +5.0 V, and +2.0 V, respectively.

to stack A and B are shown in Figure 3.4(a) and (b) respectively. When the polarization of HZO is directed away from the Al_2O_3 dielectric, the band bending in both stacks leads to a higher tunneling barrier width and thus, results in high resistance OFF state. When the polarization is directed towards the Al_2O_3, the band bending leads to a low resistance ON state. In Figure 3.1(c) and (d), it is observed that the P_R value achieved after wake-up of 2000 cycles are different for stacks A and B and this difference in the P_R value is considered in the respective band diagrams. The difference in P_R can be due to the difference in the stabilization of polarization in the two stacks due to the presence of TiO_X near the bottom electrode. In Stack A there is Al_2O_3 dielectric in the top and

TiO_X dielectric in the bottom of the HZO layer. This leads to the inability of full charge screening due to the absence of enough carriers inside the dielectrics. The band-bending is driven by the polarization inside the ferroelectric layer. The smaller P_R in stack A after wake up (6.0 $\mu C/cm^2$) leads to lesser band bending and thus leads to a larger additional tunneling barrier width across the HZO layer, marked as T_A in Figure 3.4(a). For stack A at ON state, the electrons have to tunnel across the Al_2O_3 dielectric thickness, TiO_2 thickness and some part of the HZO thickness. This leads to an increase in ON resistance and thus, a reduction in ON current in Stack A. Whereas in case of stack B, the higher P_R value of 8.5 $\mu C/cm^2$ leads to more band bending which results in a smaller tunneling barrier across the HZO layer. This is marked as T_B in Figure 3.4(b). The smaller ON state tunneling barrier width in stack B compared to stack A ($T_B < T_A$) results in its smaller ON state resistance and relatively higher ON current.

For comparing the band diagram, it is assumed that for both stacks A and B an external bias (read voltage) of -1.4 V and +1.4 V are applied on the top electrode. This was to avoid any confusion of whether the ON current difference is arising from the read voltage and to enable a fair comparison of band diagrams to understand the intrinsic difference. For the same read current magnitude, the two stacks show clear difference in the band bending as shown in Figure 3.4(a) and (b). This is due to the difference in the P_R value as well as the positioning of the individual layers. Furthermore, the broader coercive voltage distribution in stack A, limits the read voltage to -1.4 V without having the polarization state disturbed. Whereas in stack B a higher read voltage of +2.0 V could be used without affecting the reset or set state polarization. When a higher external bias is used, the band bends even more and leads to even smaller tunneling barrier width, resulting in a further increase in ON state current.

The cause for both the low P_R value and the broad coercive voltage distribution in stack A is assumed to be the presence of oxides on top and bottom of the HZO layer resulting in incomplete screening of the polarization charges. When the Al_2O_3 dielectric is placed near the bottom electrode as in stack B, both Al_2O_3 and the TiO_X are below the HZO layer. The presence of W metal in the top of HZO layer helps in stabilizing the polarization by screening the polarization charges leading to its higher remnant polarization after wake up. This higher remnant polarization, smaller coercive voltage distribution

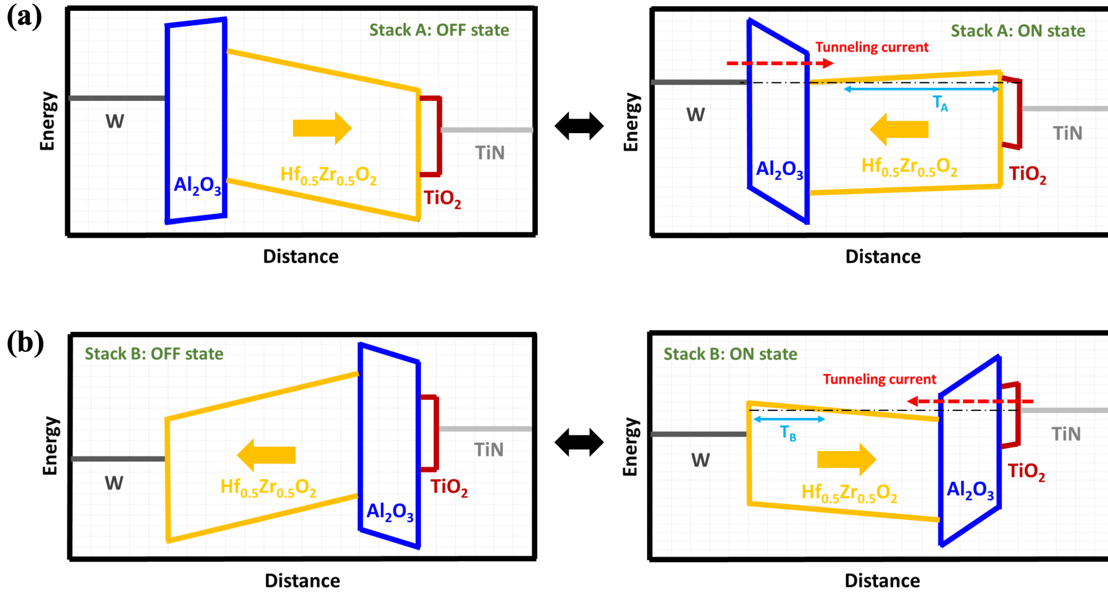

Figure 3.4: (a) The band diagram corresponding to stack A in OFF state (polarization directed away from the Al_2O_3 dielectric) and ON state (polarization directed towards the Al_2O_3 dielectric) with an external bias corresponding to the read voltage of -1.4 V applied on W electrode; (b) The band diagram corresponding stack B in OFF state and ON state by applying read voltage of +1.4 V on the W electrode. The band diagrams are generated using the "band diagram program" developed by the Knowlton research group [187, 188]. The parameters utilized for the band diagrams include the following: TiN work function = 4.45 eV, W work function = 4.5 eV, relative permittivity of HZO = 32, band gap of HZO = 5.75 eV, electron affinity of HZO = 2.7 eV, remnant polarization for stacks A = 6.0 $\mu C/cm^2$ (P_R value at 2000 cycles), remnant polarization for stacks B = 8.5 $\mu C/cm^2$ (P_R value at 2000 cycles), relative permittivity of Al_2O_3 = 9, band gap of Al_2O_3 = 8.7 eV, electron affinity of Al_2O_3 = 1.35 eV, HZO thickness = 10 nm, Al_2O_3 thickness = 3 nm, TiO_2 thickness = 1 nm, relative permittivity of TiO_2 = 80, band gap of TiO_2 = 3.5 eV, and electron affinity of TiO_2 = 2.95 eV [119, 189, 190]. The actual read voltage used for measuring OFF and ON currents in stack B is +2.0 V. For a fair comparison of band diagram, here the read voltage amplitude for both stack A and B are taken to be 1.4 V. Here, T_A is the HZO tunneling barrier width at ON state for stack A and T_B is the HZO tunneling barrier width at ON state for stack B.

and the absence of additional tunneling barrier leads to the high ON/OFF ratio for stack B compared to stack A. From this it is evident that placing the dielectric near the bottom electrode is more favorable in terms of device performance.

3.3 Effect of metal electrode positioning

The positioning of metal electrodes might change the crystallization condition as well as the interface chemistry [128, 186]. In order to understand the effect of metal positioning,

two stacks were fabricated as shown in Figure 3.5(a) and (c). For both stacks, 10 nm HZO is placed near the bottom electrode and 3 nm Al_2O_3 is placed near the top electrode. Only the position of metal electrodes is different for the two stacks. In case of stack A, 30 nm TiN metal is used as the bottom electrode and 30 nm W metal is used as the top electrode. Whereas for stack C, 30 nm W metal is used as the bottom electrode and 30 nm TiN metal is used as the top electrode. Note that, stack A was discussed in the previous section.

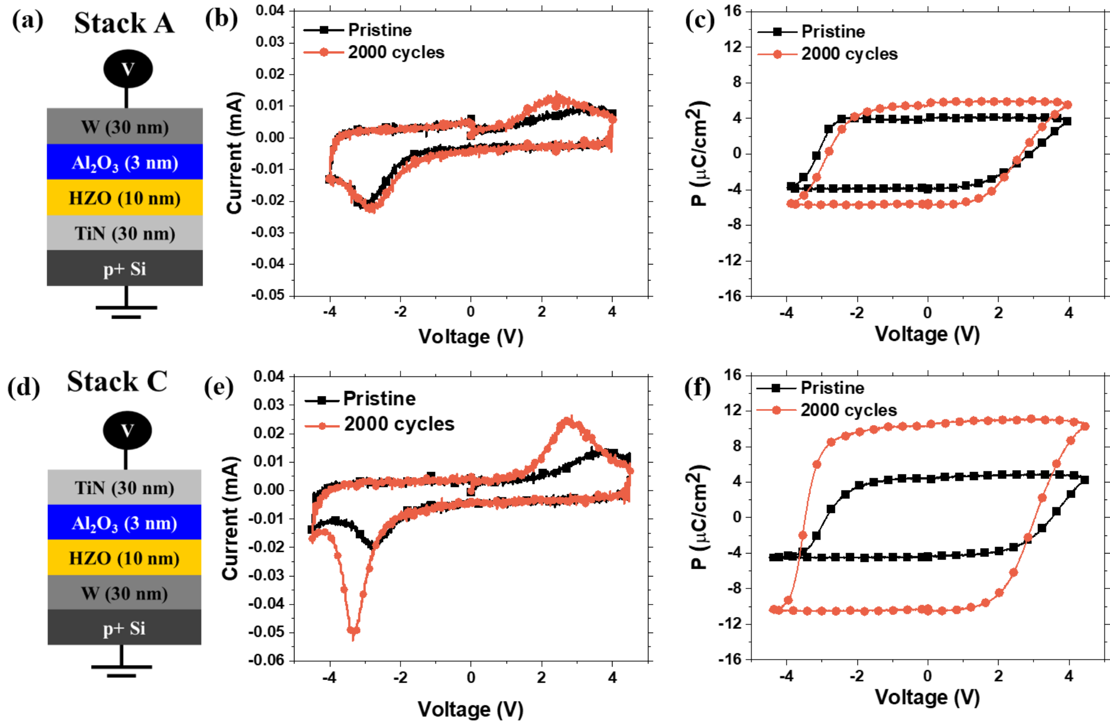

Figure 3.5: (a) Schematic of stack A, the p+Si-TiN-HZO-Al_2O_3-W FTJ device. (b) The switching I-V corresponding to stack A at pristine and wake up of 2000 cycles. (c) The PUND sequence P-V measurement corresponding to stack A at pristine and after 2000 cycles. (d) Schematic of stack C, the p+Si-W-HZO-Al_2O_3-TiN FTJ device. (e) The switching I-V corresponding to stack C at pristine and 2000 cycles. (f) The PUND sequence P-V measurement corresponding to stack B. For both the stacks, the wake-up cycling is performed with triangular pulse of 100 Hz frequency. The voltage amplitude used for wake-up cycling are $\pm$ 4.0 V, $\pm$ 4.5 V for stack A and stack C respectively. The switching I-V and P-V measurements are performed with triangular pulse of $\pm$ 4.0 V, $\pm$ 4.5 V amplitudes for stack A and C respectively and 1 ms pulse width.

The switching I-V measurements corresponding to stacks A and C are shown in Figure 3.5(b) and Figure 3.5(e) respectively. The PUND sequence P-V measurements corresponding to the stacks A and C are shown in Figure 3.5(c) and Figure 3.5(f) respectively. The maximum voltage for which the device survives switching operation and cycling operation is chosen as the maximum operating voltage. For stack A and C, the operating

voltages ($|V_{max}|$) are 4.0 V and 4.5 V respectively. The wake-up cycling operation is carried out with bipolar triangular pulse of 100 Hz frequency and V_{max} amplitude. The voltage is applied through the top electrode and the substrate is grounded. In the pristine state, both stacks show a large coercive voltage distribution and the P_R is $\sim 4\ \mu C/cm^2$. After wake-up of 2000 cycles, stack A still has a large coercive voltage distribution and P_R value only increased to $\sim 6\ \mu C/cm^2$, whereas stack C shows a much narrower coercive voltage distribution after wake-up compared to the pristine state and the P_R value is increased to $\sim 11\ \mu C/cm^2$.

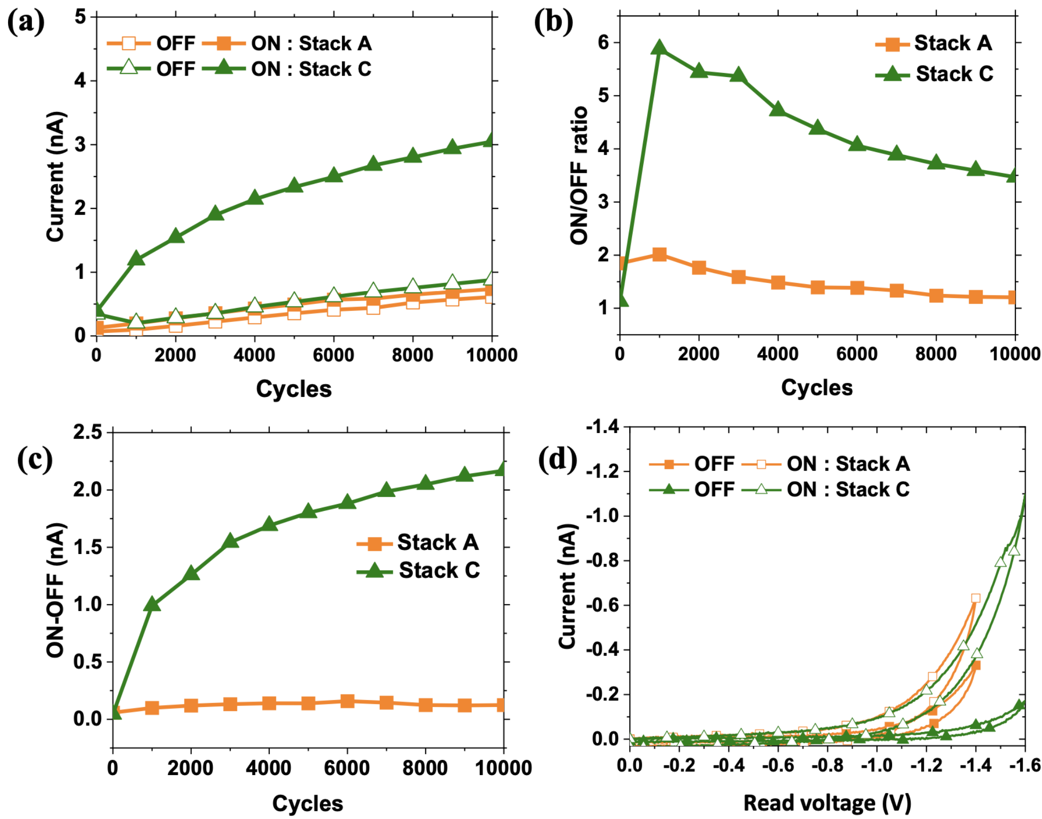

Figure 3.6: (a) Evolution ON and OFF currents from pristine to 10^4 cycles for stack A and C. (b) Evolution of ON/OFF ratio from pristine to 10^4 cycles for stack A and C (c) Evolution of ON and OFF current difference from pristine to 10^4 cycles for stack A and C. (d) Quasi-static read measurement corresponding to stack A and C after wake-up of 2000 cycles. This read I-V operation is a DC measurement where the voltage is swept quasi-statically.

The evolution of ON and OFF state currents from pristine to 10^4 cycles for stacks A and C are shown in Figure 3.6(a). For stack A, a V_{Reset} of 4.0 V and a V_{Set} of -4.0 V are used to switch the polarization to the high (OFF state) and low resistance states (ON state). The DC read voltage is -1.4 V. For stack C the reset, set, and read voltages

are 4.5 V, -4.5 V, and -1.6 V respectively. From Figure 3.6(b) we can see that stack A exhibits a low ON/OFF ratio of ∼2 and stack C has a larger ON/OFF ratio of ∼6 after 1000 cycles. Beyond 1000 cycles the ON/OFF ratio reduces for both stacks. This is due to the increase of the OFF current due to fatigue effect. The stack with higher remnant polarization shows highest ON/OFF ratio after wake-up. The difference between ON and OFF currents from pristine to 10^4 cycles are shown in Figure 3.6(c). The quasi static I-V read measurement corresponding to stacks A and C after 2000 cycles of wake-up are shown in Figure 3.6(d). Stack C shows higher ON/OFF ratio as well as higher ON-OFF current value which makes this stack more suitable than stack A.

The difference in the device performance of stacks A and C might be due to the difference in the HZO-bottom electrode interface of the two stacks. W bottom electrode does not oxidize as much as the TiN bottom electrode during the ALD deposition of HZO and Al_2O_3 layers. The Gibb's free energy of formation for WO_x is larger compared to that of TiO_x and this leads to less interfacial reaction or oxygen scavenging at the W/HZO interface compared to TiN/HZO interface [191, 192]. The relatively thin interfacial oxide at HZO-W interface leads to better stabilization of the polarization through charge screening and to the absence of an additional tunneling barrier. Thus, Stack C shows higher P_R, ON/OFF ratio and ON-OFF current.

To confirm this, hard X-ray photoelectron spectroscopy (HAXPES) measurements were conducted on stacks A and C. Photoelectron spectroscopy is sensitive to local chemistry, but the typical probing depth using soft X-rays is only a few nm [193]. With hard X-rays, using synchrotron radiation, HAXPES is a powerful tool to study local chemical changes at buried interfaces as the inelastic mean free path (IMFP) for the same core level electrons increases and, hence, the probing depth by up to an order of magnitude [193]. After removing the 30 nm thick top electrodes via chemical etching, the samples were introduced in the ultrahigh vacuum HAXPES chamber of the P22 beamline at the DESY synchrotron, Germany [194]. We have investigated the Ti 2p and W 4f core levels to evaluate the oxidation state of the bottom electrode material near the interface. The analysis of the spectra was performed by Dr. Wassim Hamouda.

Figure 3.7 shows the fitted spectra recorded at 7.6 keV photon energy with a take-off angle of 75°. The inelastic mean free paths (IMFPs: λ) of the Ti 2p and W 4f electrons

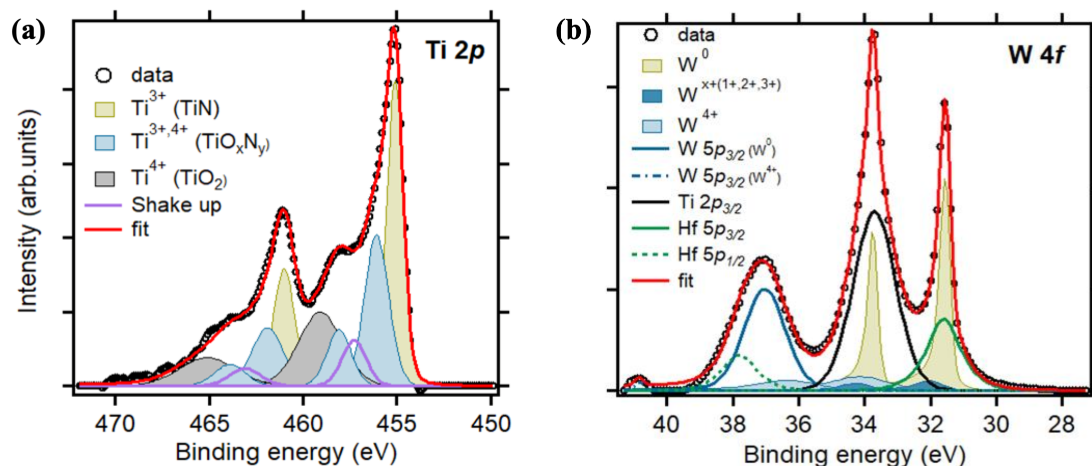

Figure 3.7: (a) Ti 2p and (b) W 4f HAXPES core level spectra recorded from stacks A and C, respectively, using 7.6keV photon energy. The HAXPES measurements were conducted by Dr. Florian Maudet (postdoctoral fellow at QM-IFOX, HZB) and Zora Chalkley at the DESY synchrotron. The analysis was carried out by Dr. Wassim Hamouda (postdoctoral fellow at QM-IFOX, HZB).

across the HZO and the alumina layers using these experimental conditions are calculated using the Tanuma, Powell, and Penn (TPP-2M) algorithm to be ∼10 nm [195]. The sampling depths, defined as 3λ, are therefore ∼30 nm. Figure 3.7(a) shows the Ti 2p core level recorded for stack A. It can be fitted with five spin-orbit doublets. The first one located at the lowest binding energy at 455.1 eV (Ti $2p_{3/2}$) corresponds to Ti^{3+} from TiN metallic environment. The three other doublets, situated at higher binding energy, correspond to a higher oxidation of Ti. The contribution from the two peaks shown in blue color are related to oxynitride phases ($Ti^{3+,4+}O_xN_y$) while the one at the highest binding energy (shown in grey) can be unambiguously attributed to Ti^{4+} environment indicating the presence of TiO_2 phase (Ti $2p_{3/2}$ at 459.1 eV). The spectrum also includes a shake-up satellite component related to TiN, constrained at 1.9 eV higher energy with respect to the metallic Ti $2p_{3/2}$. This contribution originates from the kinetic energy loss due to the interaction of the photoelectron with a valence electron. The overall fitting procedure agrees very well with previous reported analyses on TiN [196, 197].

For the stack C, Figure 3.7(b) shows the recorded W 4f spectrum which, similarly, originates only from the bottom electrode. The result shows the presence of metallic contribution (W^0) at the lowest binding energy and of oxidized phases WO_x related to W^{x+} (1+,2+,3+ and 4+) [198]. However, there is no evidence of a higher oxidation state in W^{6+}

for instance related to WO_3 contribution. The spectrum also includes other transitions, which occur in the same energy window and are shown in solid lines. This is the case of the spin-orbit doublet from Hf 5p (in green), W $5p_{3/2}$ (in blue) and Ti $2p_{3/2}$ electrons (in black) [199]. The latter is due to residual TiN remaining at the top of the sample due to the incomplete chemical etching. Now, by comparing the oxides and sub-oxides areas relative to the total peak area in each case (I_{oxides}/I_{total}), we found that the TiN electrode presents 54% of oxidized environment while the W one presents only 23%. This can be explained by the more negative Gibbs free energy for titanium oxides formation with respect to tungsten ones. So, during the first steps of the ALD cycles, the oxygen supply would oxidize the TiN layer in a higher amount compared to W. It is important to mention that there was a break in the process, with air exposure occurring between the deposition of the bottom electrode and the HZO layer.

We therefore attribute the higher $\mathrm{P_R}$ in stack C to the better screening efficiency of the polarization charges with W as BE. In addition, it is possible that the different interfacial tungsten sub-oxides may be even metallic which is not the case for $\mathrm{TiO_2}$ [200]. The only case where Ti sub-oxide may be conductive is the $\mathrm{Ti_4O_7}$ Magneli phase forming conductive nanofilaments and exploited in $\mathrm{TiO_2}$-based resistive switching [201]. However, as shown from our HAXPES data, this is unlikely happening. The presence of an insulating $\mathrm{TiO_2}$ interface layer would cause a higher effective screening length (λ_{eff}) between the polarization and the electrode screening charges resulting in significant voltage drop, higher depolarizing field and lower polarization value.

3.4 Optimum FTJ Stack

Building upon the discussions in earlier sections, we have established that the location of the dielectric and the arrangement of the metal electrodes significantly influence the performance of the FTJ devices. Figure 3.8 presents the schematics, switching I-V, and PUND P-V, while Figure 3.9 illustrates the ON, OFF currents versus cycles and ON/OFF ratio versus cycles, showcasing the FTJ electrical characteristics of the different stacks investigated. The comparison of the characteristics of stack A and B indicates that placing the dielectric near the bottom electrode leads to enhanced switching, increased remnant polarization post wake-up, and a higher ON/OFF ratio (discussed in Section 3.2).

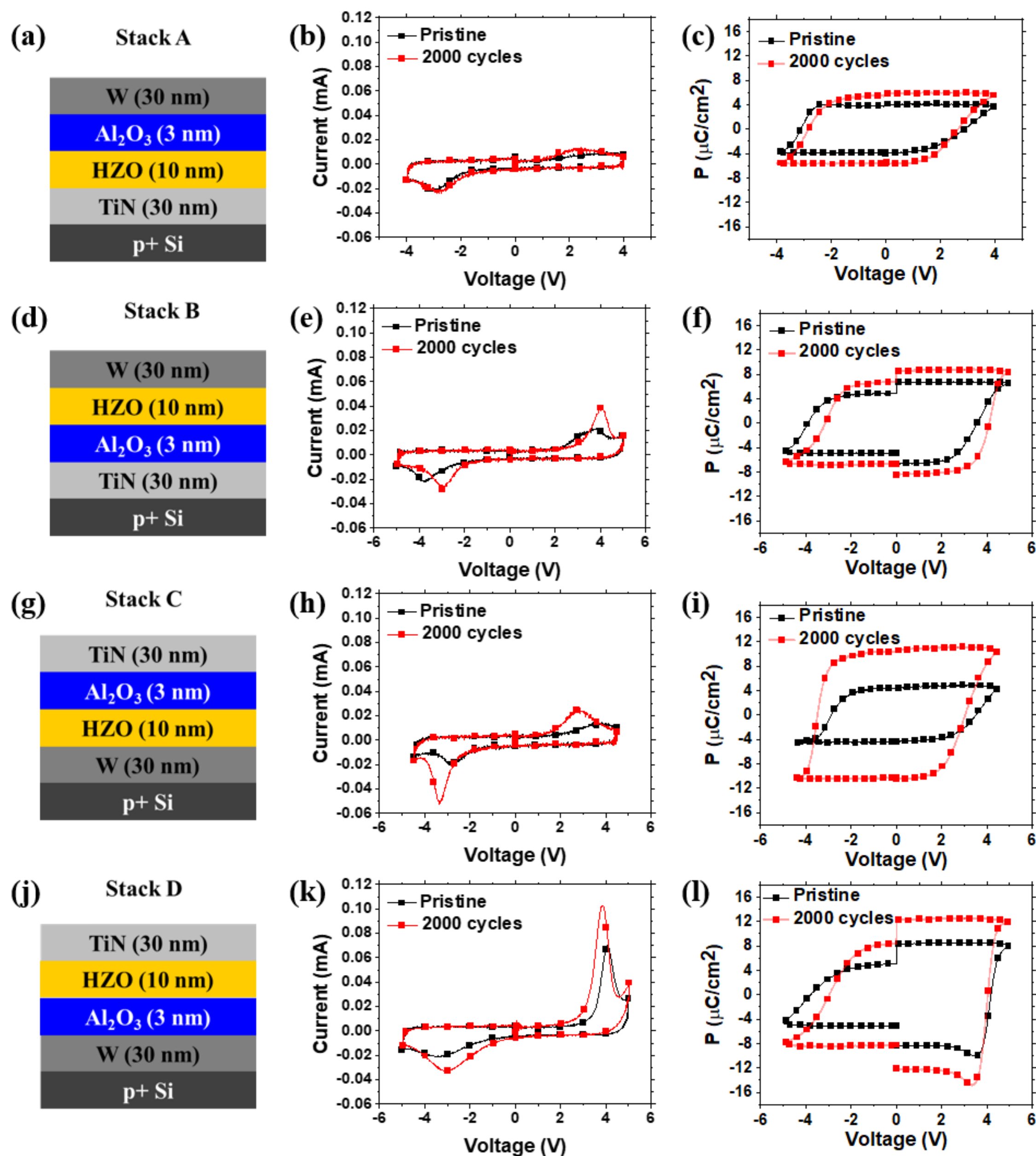

Figure 3.8: Comparison of four different device architectures labeled as stacks A, B, C, and D, each varying in dielectric and electrode placement. Switching I-V and P-V for stack A, both at pristine and after 2000 cycles, are depicted in (b) and (c). Switching I-V and P-V for stack B at pristine and after 2000 cycles are shown in (e) and (f). For stack C, switching I-V and P-V at pristine and 2000 cycles are illustrated in (h) and (i). Finally, switching I-V and P-V for stack D at pristine and 2000 cycles are presented in (k) and (l), where wake-up cycling in Stack D is performed with a triangular waveform of 100Hz frequency and ±5.0 V amplitude and measurements are taken with a triangular pulse of ±5.0 V amplitude and 1 ms pulse-width.

Similarly, a comparison between stack A and C reveals that FTJ device with W electrode positioned as the bottom electrode and TiN as the top electrode yields higher remnant polarization, translating to a superior ON/OFF ratio after wake-up (discussed in Section 3.3).

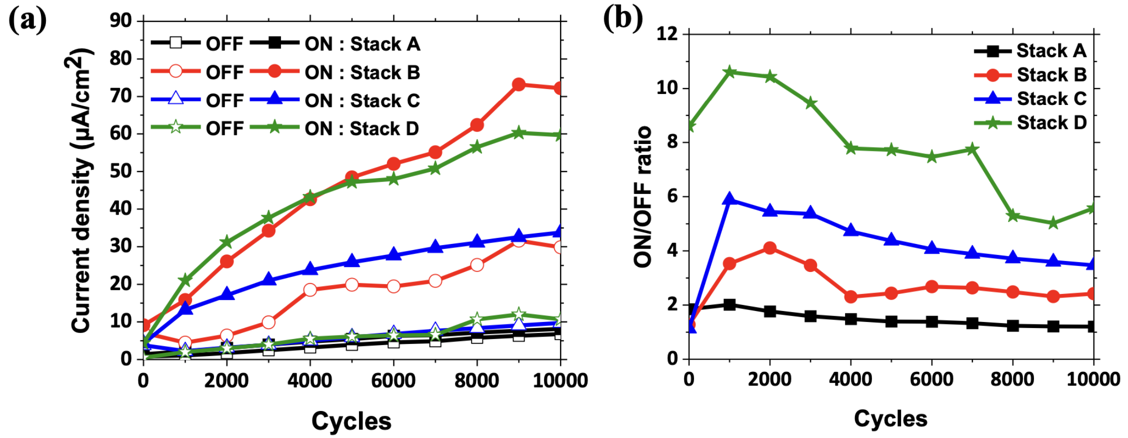

Figure 3.9: (a) Evolution ON and OFF current density from pristine to 10^4 cycles for stack A, B, C and D. (b) Evolution of ON/OFF ratio from pristine to 10^4 cycles for stack A, B, C and D. The OFF and ON currents are measured after switching the polarization to OFF and ON states through monopolar triangular reset and set pulses. The reset pulse used for stack A, B, C and D have an amplitude of +4.0 V, -5.0 V, +4.5 V and -5.0 V respectively and monopolar pulse width of 0.5 ms. Whereas the set pulse have amplitudes -4.0 V, +5.0 V, -4.5 V and +5.0 V respectively and monopolar pulse width of 0.5 ms. The read measurements are carried out by applying DC voltages of -1.4 V, +2.0 V, -1.6 V and +1.8 V respectively.

Based on these insights, we fabricated a FTJ device with the stack architecture depicted in Figure 3.8(j) as stack D. This device combines the advantages of having the dielectric near the bottom electrode and utilizing W as the bottom electrode, with TiN serving as the top electrode. In stack D, both the bottom and top electrodes are patterned with liftoff process as discussed in Section 2.4.3. The bottom electrode measures $110 \times 200\ \mu m^2$, while the top electrode measures $100 \times 100\ \mu m^2$. Additionally, a 30nm W layer is incorporated above the top TiN electrode in stack D to prevent oxidation of the top electrode.

As anticipated, stack D exhibits optimal performance in terms of remnant polarization, ON current, and ON/OFF ratio. As the dielectric is positioned near the bottom electrode in stack D, it becomes feasible to lift off the top electrode without the risk of etching away Al_2O_3 layer in the developer solution. Therefore, stack D offers process simplicity to in-

tegrate it onto the CMOS back-end-of-line (BEOL) in our laboratory process. Therefore, it is selected for integration into the CMOS BEOL, as elaborated in Chapter 6.

3.5 Effect of dielectric thickness

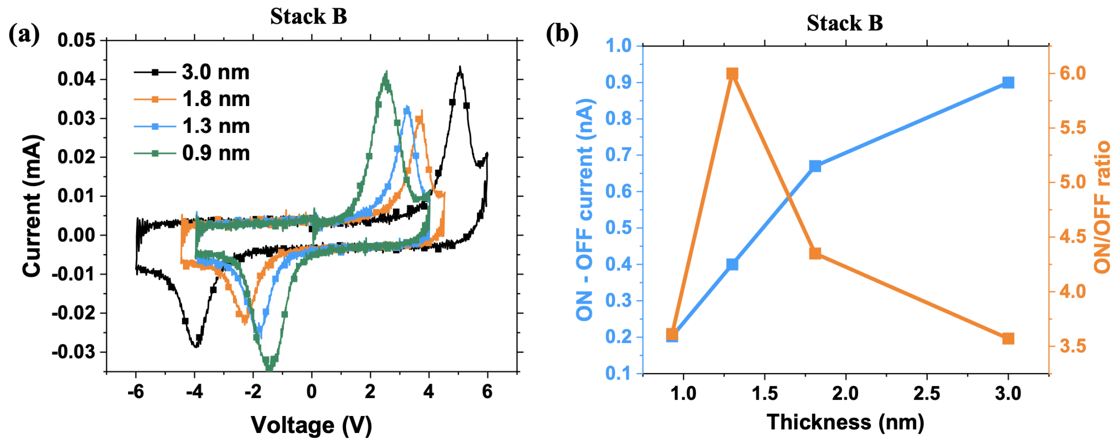

Figure 3.10: (a) Switching I-V for FTJ devices with stack B architecture and Al_2O_3 thickness varying from 0.9 nm to 3.0 nm after wake-up (2000 cycles). (b) Comparison of ON/OFF ratio and difference between ON and OFF currents for different thicknesses of dielectric in case of stack B FTJ. The read voltages are +1.3 V, +1.6 V, +1.8 V and +2.5 V for the FTJ stacks with 0.9 nm, 1.3 nm, 1.8 nm and 3.0 nm dielectric thicknesses. The wake-up cycling is performed with triangular waveform of 100 Hz frequency. The voltage amplitude used for the wake-up and switching measurements are 4.0 V, 4.0 V, 4.5 V and 6.0 V for dielectric thickness 0.9 nm, 1.3 nm, 1.8 nm and 3.0 nm respectively. For the switching I-V measurement, the pulse width used is 1 ms.

The impact of the Al_2O_3 dielectric thickness on the polarization switching behavior for devices with stack B architecture is shown in Figure 3.10(a). As the dielectric thickness increases, the coercive voltage associated with the switching peak also increases. This occurs because a greater portion of the applied voltage drops across the thicker dielectric layer, necessitating an increase in the applied voltage to achieve the required coercive electric field across the ferroelectric material.Thus, different voltages ($\pm V_{max}$) are used for each of these thicknesses in-order to perform switching operation. V_{max} is the highest voltage the device survives for switching and cycling operations. The FTJ device performance of these stacks are shown in Figure 3.10(b). The reset and set voltages for each thickness are determined based on the I-V switching behavior. A voltage of $-|V_{max}|$ is applied as the reset voltage, while $+|V_{max}|$ serves as the set voltage. The read

voltages are set at +1.3 V, +1.6 V, +1.8 V, and +2.5 V for the FTJ stacks with dielectric thicknesses of 0.9 nm, 1.3 nm, 1.8 nm, and 3.0 nm, respectively. The stack with 1.3 nm of Al_2O_3 shows the highest ON/OFF ratio of ~6. But it only has a ON-OFF current of 0.4 nA. Hence it is less suitable for attaining multiple resistance states. In case of 3 nm thick dielectric, the ON/OFF ratio is ~ 3.5 but it has higher ON – OFF current value of ~0.9 nA.

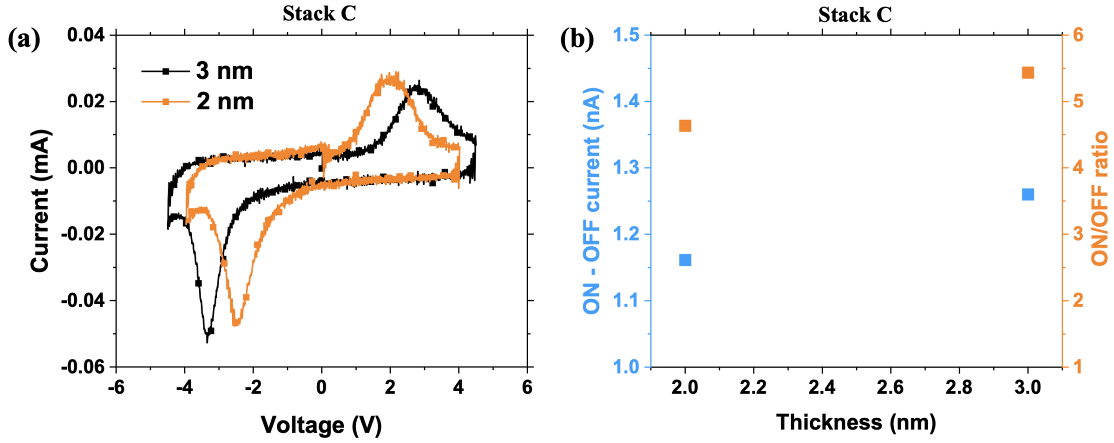

Figure 3.11: (a) Switching I-V measurement of FTJ devices with stack C architecture and Al_2O_3 thicknesses of 2 nm and 3 nm after wake-up (2000 cycles). (b) Comparison of ON/OFF ratio and difference between ON and OFF currents for the two thicknesses of dielectric in case of stack C FTJ. The read voltages are -1.5 V and -1.6 V for the FTJ stacks with 2.0 nm and 3.0 nm dielectric thicknesses. The wake-up cycling is performed with triangular waveform of 100 Hz frequency. The voltage amplitude used for the wake-up and switching measurements are 4.0 V and 4.5 V for dielectric thickness 2.0 nm and 3.0 nm respectively. For the switching I-V measurement, 1 ms pulse width is used.

The impact of dielectric thickness on the switching characteristics of FTJ devices with stack C architecture is shown in Figure 3.11(a). As expected, the stack with 2 nm Al_2O_3 switches with a lower voltage compared to the stack with 3 nm Al_2O_3. The ON/OFF ratio and ON-OFF characteristics of these stacks are shown in Figure 3.11(b). For these stacks, +$|V_{max}|$ serves as the reset voltage, and -$|V_{max}|$ is used as the set voltage. Read voltages of -1.5 V and -1.6 V are chosen for stacks with dielectric thicknesses of 2 nm and 3 nm, respectively. The ON/OFF ratio for both thicknesses is approximately 5, with the ON-OFF current falling in the range of approximately 1 nA for both stacks. Both stacks exhibit similar performance characteristics.

3.6 Impact of sample processing

In this section we discuss how the process flow for fabricating FTJ devices impacts the device performance. A bilayer FTJ stack with p+Si-TiN-HZO-Al_2O_3-W architecture was fabricated in two different ways as shown in Figure 3.12.

The ”stack anneal top (SAT)” FTJ stack (Figure 3.12(a)) was fabricated by depositing a 30 nm TiN metal layer through sputtering onto a p+Si substrate. Next, 10 nm of HZO and 3 nm of Al_2O_3 layers are deposited through ALD deposition. This is followed by sputtering of a 30 nm W layer as the top metal. After the blanket deposition of W metal, the stack was annealed in RTP at 400 °C for 120 s in an N_2 atmosphere to crystallize the HZO layer into the ferroelectric orthorhombic phase. Then, the top electrode was patterned using photo-lithography and lift-off processes which involved Ti (10 nm) and Pt (100 nm). Finally, the W metal was selectively etched outside of the pad area using peroxide (H_2O_2) solution at 50°C. The device’s name suggests that in this stack, the crystallization anneal was performed after the deposition of all layers in the M-FE-DE-M stack.

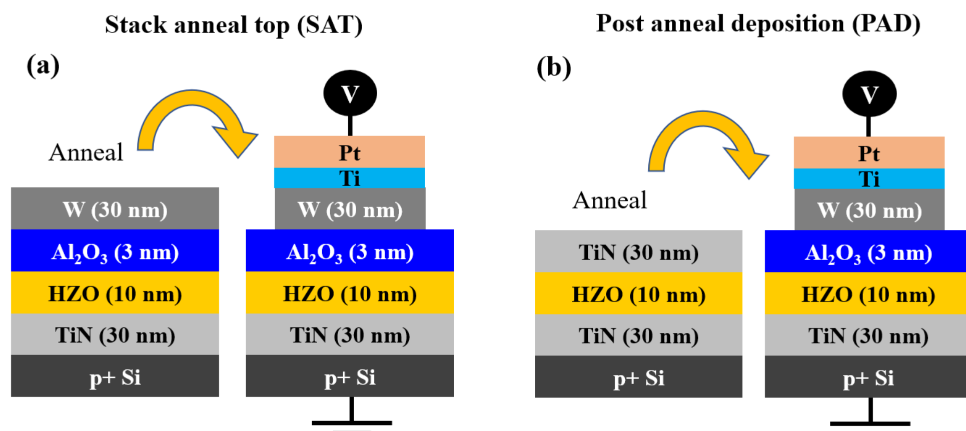

Figure 3.12: (a) Schematic of stack anneal top (SAT) device. Here the HZO crystallization annealing is done on the M-FE-DE-M stack and then the top electrode is patterned by Ti (10nm)/Pt (100nm) lift off and W wet etch. (b) Schematic of post anneal deposition (PAD) device. Here the HZO is crystallized by annealing TiN-HZO-TiN stack. Then the TiN top electrode is removed by wet etching and Al_2O_3 and W top electrode are deposited. Later the top electrode is patterned by Ti (10nm)/Pt (100nm) lift off and W wet etch. For both the stacks, HZO crystallization is done with RTP of 400 °C, 120 s in N_2 atmosphere.

Whereas ”post anneal deposition (PAD)” FTJ stack as shown in Figure 3.12(b) is fabricated by first depositing 30 nm TiN metal, 10 nm HZO and 30 nm TiN on p+Si sub-

strate. Here the HZO crystallization anneal of 400 °C, 120 s with RTP at N_2 atmosphere is performed on the TiN-HZO-TIN M-FE-M stack. After annealing, the top TiN metal is etched with SC1 solution at 50 °C. Then, 3 nm Al_2O_3 and 30 nm W is deposited. The top W electrode is patterned with lift off of Ti (10 nm)/Pt (100 nm) followed by wet etching with peroxide solution at 50 °C. The main difference between the two stacks is that in SAT stack the crystallization annealing is done on the entire M-FE-DE-M stack and in PAD stack the crystallization anneal is done on M-FE-M stack where the dielectric layer is deposited after the anneal. Thus, the dielectric layer and the top W electrode have not encountered the 400 °C crystallization anneal in PAD stack.

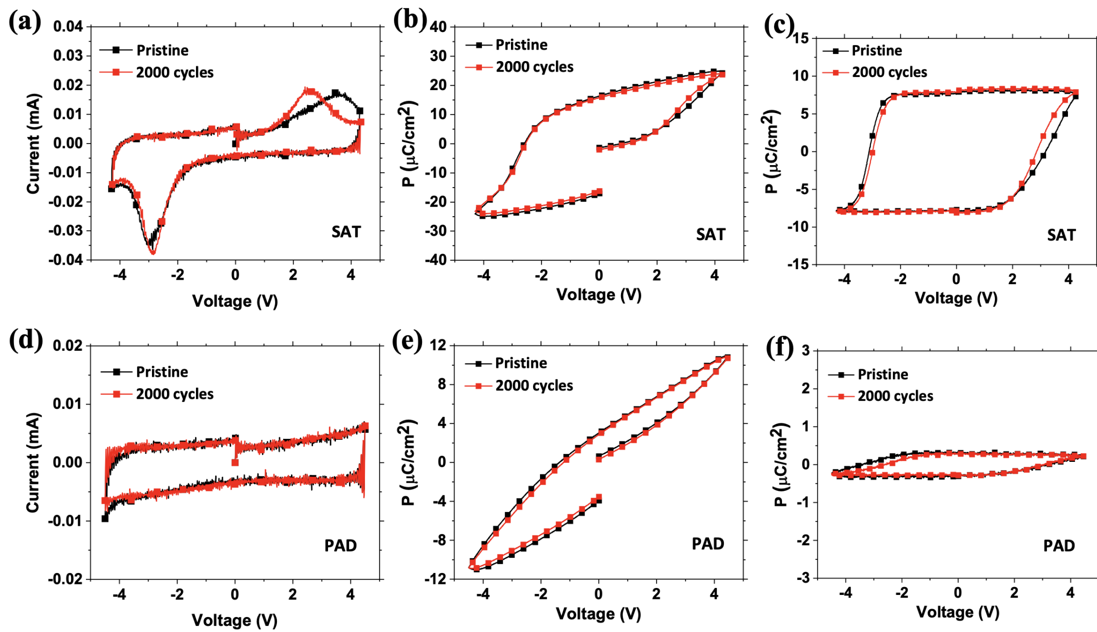

Figure 3.13: (a) Switching I-V, (b) P-V and (c) PUND sequence P-V measurement corresponding to pristine and wake-up state of 2000 cycles for SAT device. Here the polarization is switched with triangular pulse of ±4.3 V, 1 ms and the wake-up cycling is performed with triangular waveform of ±4.0 V and 1 kHz frequency. This stack does not survive wake-up cycling with voltage higher than 4.0 V. (d) Switching I-V, (e) P-V and (f) PUND sequence P-V measurement corresponding to pristine and wake-up state of 2000 cycles for PAD device. Here the polarization is switched with triangular pulse of ±4.5 V, 1 ms and the wake-up cycling is performed with triangular waveform of ±4.5 V and 1 kHz frequency.

The electrical characterization results corresponding to the two stacks are shown in Figure 3.13. The switching I-V, P-V and PUND sequence P-V measurements corresponding to SAT stack is shown in Figure 3.13(a), (b) and (c) respectively. Here the polarization is switched with ±4.3 V and the wake-up cycling is performed with triangular waveform

of ±4.0 V and 1 kHz frequency. In SAT stack, ferroelectric switching is observed from pristine state. After wake up of 2000 cycles, the positive coercive voltage peak shifts to lower voltage and there is no major change in the position of negative coercive voltage peak other than the narrowing of the coercive voltage distribution. From the P-V measurement and the PUND sequence P-V measurement we can see that the there is no significant increase in the PR from pristine to 2000 cycles. The stack shows a P_R of ~8 $\mu C/cm^2$. The switching I-V, P-V and PUND sequence P-V measurements corresponding to PAD stack are shown in Figure 3.13(d), (e) and (f) respectively. Here the polarization is switched with ±4.5 V and the wake-up cycling is performed with triangular waveform of ±4.5 V and 1 kHz frequency. However, in this stack, we do not observe any signature of polarization switching in either the I-V or P-V measurements, both at pristine or after 2000 cycles, despite the applied voltage being slightly higher than the switching voltage used in the case of the SAT stack. The absence of switching peaks in I-V measurements and the low remnant polarization of ~ 0.5 $\mu C/cm^2$ indicates that no polarization can develop in the HZO layer. This can be due to different reasons. Either the crystallization of the polar phase of HZO has not occurred or the Al_2O_3-HZO interface is different from that of SAT stack and can not provide enough screening charges.

To confirm the crystallization of the HZO layer into the ferroelectric phase in the PAD stack, we conducted switching measurements solely on the HZO layer. For this purpose, photolithography was performed on the PAD sample outside the W pad areas, and the Al_2O_3 layer was etched in a square pad shape using resist developer AZ726 MIF. Subsequently, a 30 nm W metal was lifted off in that space. This modified stack type is referred to as PAD-MIM, indicating an M-FE-M stack within the PAD sample. The stack architecture is illustrated in Figure 3.14(a). The electrical measurements were performed by applying voltage on the top electrode and by grounding the chuck. The switching I-V, P-V and PUND sequence P-V measurements corresponding to PAD-MIM stack is shown in Figure 3.14(b), (c) and (d) respectively. Here the polarization is switched with triangular voltage pulse of ±2.7 V and 1 ms pulse width. The wake-up cycling is performed with triangular waveform of ±2.7 V and 1kHz frequency. We observe that the polarization switching occurs from the pristine state onwards. There is no increase in remnant polarization from pristine to 10000 cycles. The PAD-MIM stack shows a P_R of

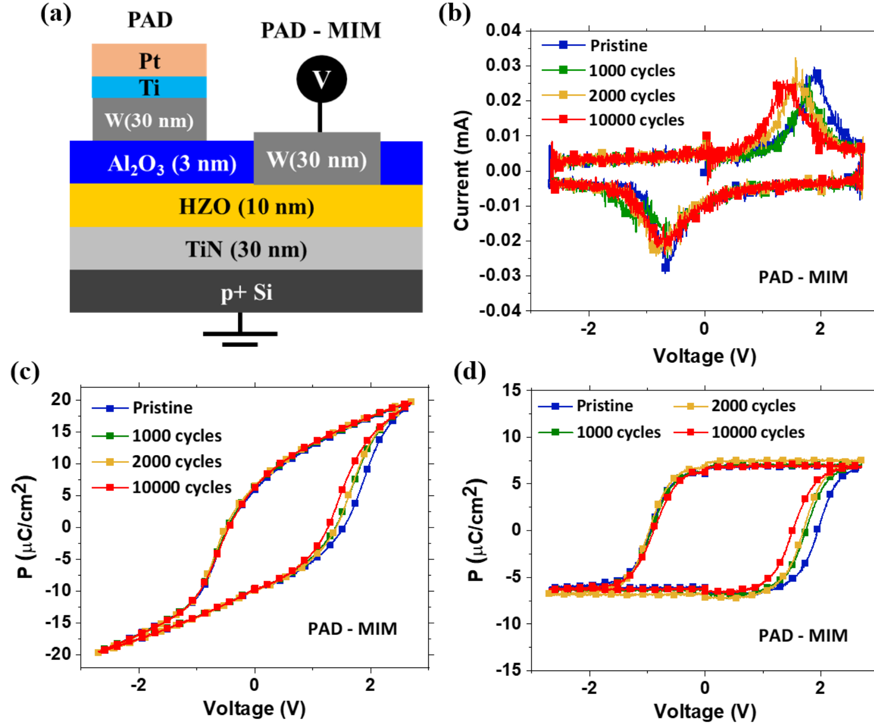

Figure 3.14: (a) Schematic of PAD-MIM stack fabricated on the same sample that has the PAD devices. Here, lithography is done to etch the $\mathrm{Al_2O_3}$ in square pad of 95x95 μm from outside PAD device area and 30 nm W is lifted off in this region. (b) Switching I-V, (c) P-V and (d) PUND sequence P-V measurement corresponding to pristine, 1000, 2000 and 10000 cycles for PAD-MIM device. Here the polarization is switched with triangular pulse of $\pm$2.7 V, 1 ms and the wake-up cycling is performed with triangular waveform of $\pm$2.7 V and 1 kHz frequency.

$\sim 7\ \mu\mathrm{C/cm^2}$. This value is significant (showing the presence of a polar phase) but lower than the one typically measured in a M-FE-M stack.

For comparison, another stack similar to PAD-MIM is fabricated on p+ Si substrate. We call this new stack MIM and it is shown in Figure 3.15(a). 30 nm TiN metal was sputtered on top of p+ Si substrate followed by ALD deposition of 10 nm HZO and sputtering deposition of 30 nm of W metal. The stack is annealed in RTP at 400 °C, 120 s in N_2 atmosphere. The switching I-V, P-V and PUND sequence P-V measurements are shown in Figure 3.15(b), (c) and (d) respectively. From the I-V measurement corresponding to pristine state, the coercive voltage distribution is very broad. With wake-up cycles the coercive voltage becomes more symmetric and the coercive voltage distribution narrows in both positive and negative polarities. After wake-up, the remnant polarization is $\sim$ 15 $\mu\mathrm{C/cm^2}$. This value is much larger than that in the PAD-MIM stack after wake-up. This could be due to incomplete etching of the $\mathrm{Al_2O_3}$ layer before the lift-off of the top metal,

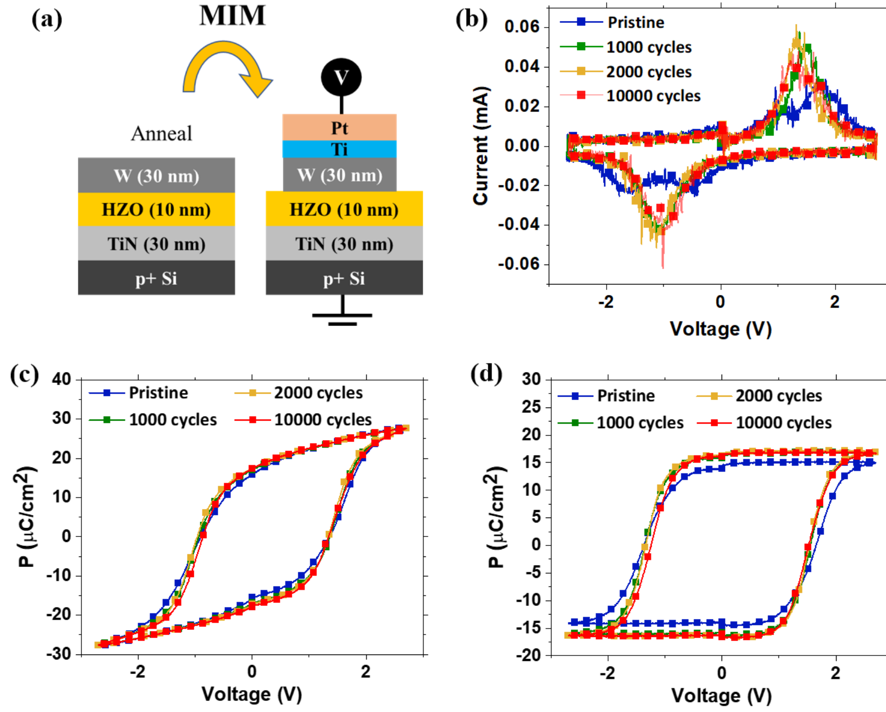

Figure 3.15: (a) Schematic of the MIM stack with TiN-HZO-W architecture. The stack is annealed with RTP of 400 °C, 120 s in N_2 atmosphere. Then the top electrode is patterned by Ti/Pt lift off followed by W wet etch. (b) Switching I-V, (c) P-V and (d) PUND sequence P-V measurement corresponding to pristine, 1000, 2000 and 10000 cycles for MIM device. Here the polarization is switched with triangular pulse of ±2.7 V, 1 ms and the wake-up cycling is performed with triangular waveform of ±2.7 V and 1 kHz frequency.

potentially leaving a thin Al_2O_3 layer with an unknown thickness at the HZO-W interface of the PAD-MIM device. However, it is clear from the electrical measurement on PAD-MIM sample that the HZO is ferroelectric and it indeed does switch in the absence of thick Al_2O_3 layer of ~3 nm thickness. The FTJ stack demonstrates polarization switching when the 3 nm Al_2O_3 layer is annealed. Based on this observation, we anticipate being able to induce polarization switching in the PAD stack if the thickness of Al_2O_3 is less than ~3 nm.

The PAD stack was also created with Al_2O_3 thicknesses of 2.5 nm and 2 nm, depicted in Figure 3.16(a). The switching I-V and P-V measurements for Al_2O_3 thickness of 2.5 nm and 2.0 nm are shown in Figure 3.16(b), (c) and Figure 3.16(d), (e) respectively. The PUND P-V measurement resulted in oxide breakdown due to the application of multiple standard bipolar pulses as part of the PUND sequence, as discussed in Section 2.5.3; hence, it is not displayed here. When the Al_2O_3 thickness is 2.5 nm, the pristine state

exhibits a broad coercive voltage distribution, which narrows after 2000 cycles. Similarly, in the stack with 2.0 nm Al_2O_3, switching characteristics are observed from the pristine state. After 2000 cycles, the coercive voltage distribution narrows compared to the pristine state, and the magnitude of the switching peak current increases. Thus, in the PAD stack with a 2.0 nm thick dielectric layer, clear evidence of polarization switching is observed. However, in the stack with a 2.5 nm thick dielectric, although switching occurs from the pristine state, the stack has a lower remnant polarization compared to the stack with a 2.0 nm thick dielectric layer.

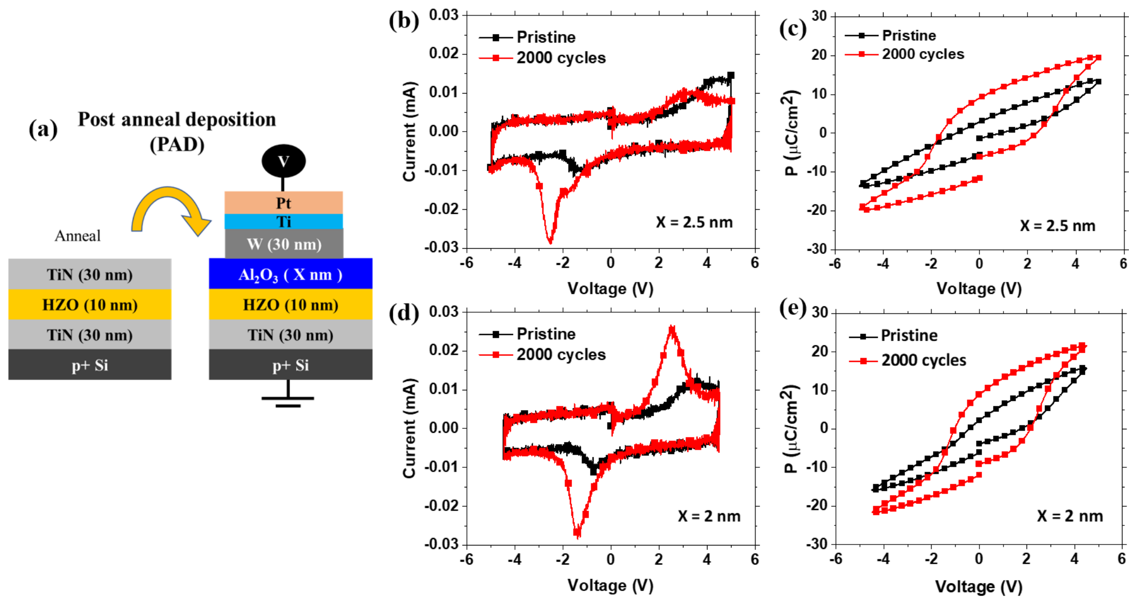

Figure 3.16: (a) Schematic representation of post anneal deposition (PAD) stack with Al_2O_3 thickness as X nm. Here the HZO crystallization is performed on TiN-HZO-TiN stack and then the top TiN is removed and Al_2O_3 layer and W top electrode are deposited and patterned through Ti/Pt lift off followed by W etching. (b) Switching I-V and (c) P-V measurement corresponding to pristine and 2000 cycles for PAD device with Al_2O_3 thickness of 2.5 nm. (d) Switching I-V and (e) P-V measurement corresponding to pristine and 2000 cycles for PAD device with Al_2O_3 thickness of 2.0 nm. For 2.5 nm Al_2O_3 thickness, the polarization is switched with triangular pulse of $\pm$5.0 V, 1 ms and the wake-up cycling is performed with triangular waveform of $\pm$5.0 V and 1 kHz frequency. For 2.0 nm Al_2O_3 thickness, the polarization is switched with triangular pulse of $\pm$4.5 V, 1 ms and the wake-up cycling is performed with triangular waveform of $\pm$4.5 V and 1 kHz frequency.

In PAD stack, the Al_2O_3 layer is not annealed with HZO layer as in the case of SAT stack. Our hypothesis is that when the HZO and Al_2O_3 are annealed together, enough charge traps are generated around the HZO-Al_2O_3 interface which facilitates the stability of polarization by screening the polarization charges and enables the switching of polar-

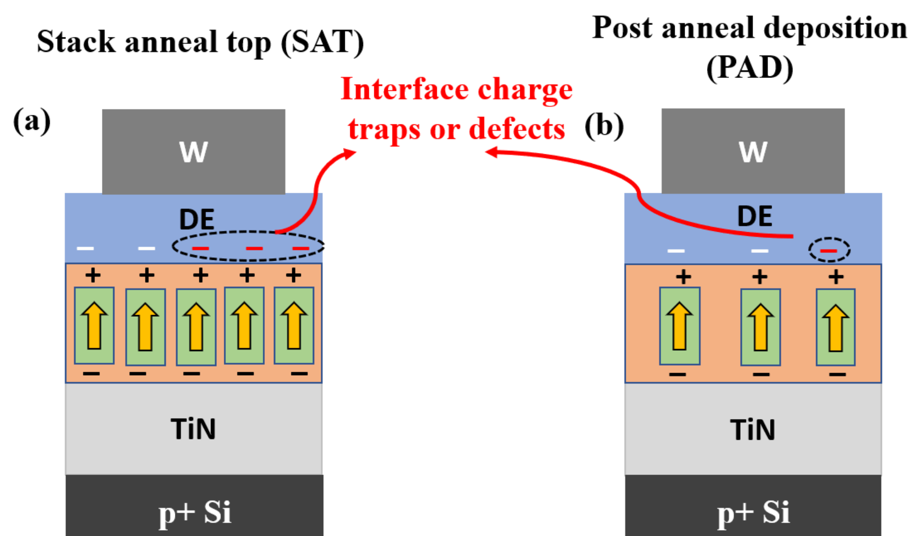

Figure 3.17: Schematic representation of the difference in remnant polarization in (a) SAT device and (b) PAD device. The interface charge traps or defects in the HZO-Al_2O_3 interface produced during the stack annealing of SAT device, helps to stabilize the domains by screening the polarization charge. This leads to high remnant polarization. Where as in PAD stack, there are not enough charge traps to stabilize the polarization.

ization. This charge trap generation could also involve change in ionic concentration (for e.g. oxygen vacancies) in the layers/near the interface, which may also become sources of charge traps. When the Al_2O_3 layer is not annealed with HZO, not enough charge traps are present around the HZO-Al_2O_3 interface and due to this reason, remnant polarization does not develop (or can't be stabilized) in the stack with 3 nm Al_2O_3. When the Al_2O_3 thickness is less, the charge traps are still less compared to SAT stack, but the top electrode is probably able to screen polarization charge through the thin dielectric layer. A schematic representation of our hypothesis is shown in Figure 3.17. In case of SAT stack there are more interface defects or charge traps developed during the crystallization of HZO-Al_2O_3 bilayer stack as shown in Figure 3.17(a). This helps in the compensation of the ferroelectric charges and leads to low depolarization field. Thus, there is a high remnant polarization. In contrast, in the PAD stack (the Al_2O_3 layer in the stack has not been annealed), there is a low concentration of interface charge traps as shown in Figure 3.17(b) and this leads to high depolarization field and low remnant polarization.

According to our hypothesis, annealing the HZO-Al_2O_3 layers together creates more charge traps, at or near the interface, and leads to stabilization of the polarization. To confirm this hypothesis, the PAD stack with 3 nm Al_2O_3 was annealed again by RTP

at 400 $^{\circ}$C, 120 s in N_2 atmosphere. This sample also contains PAD-MIM stacks. The switching I-V and PUND sequence P-V measurements at 2000 cycles, corresponding to the PAD stack before and after the re-annealing are shown in Figure 3.18(a) and (b) respectively. We observe that after re-annealing the sample, PAD stack shows polarization switching with a remnant polarization value of $\sim 8\ \mu\mathrm{C/cm^2}$. This is similar to the polarization obtained in the SAT stack after wake-up of 2000 cycles (shown in Figure 3.18(b)). Note that prior to re-annealing, no polarization switching was observed even after 2000 cycles. Hence, the measurement and observation support our hypothesis that annealing the $\mathrm{Al_2O_3}$-HZO layer together generate charge traps that are necessary for stabilizing the polarization. However, it's possible that the re-annealing process has induced crystallization of additional ferroelectric orthorhombic domains, altering the HZO layer itself in the PAD-MIM stack. Therefore, the reference PAD-MIM stack is also re-annealed and I-V, PUND sequence P-V measurements post re-annealing are shown in Figure 3.18(c) and (d) respectively. The switching I-V curves, look very similar before and after the re-annealing. There is a minor increase in the $\mathrm{P_R}$ value by $\sim 1\ \mu\mathrm{C/cm^2}$ after re-annealing. Therefore, it seems that there is no significant increase in ferroelectric HZO phase. Hence, we conclude that the component which majorly changed after the re-annealing in PAD stack is the $\mathrm{Al_2O_3}$ – HZO interface and the amount of charge traps.

The observation indicates that charge traps are highly necessary for stabilizing the polarization and play a crucial role in switching mechanism in bilayer FTJ stacks. In case of $\mathrm{Al_2O_3}$ as the dielectric, we observed that it needs to be annealed in order to have the necessary charge traps and hence the PAD process is not suitable. However, if we use a dielectric with higher amount of charge traps in as deposited condition, we may be able to attain polarization switching with PAD process even with a dielectric thickness of 3 nm. To confirm this, we fabricated PAD stack with $\mathrm{GaO_x}$ (PAD-$\mathrm{GaO_x}$) of 3 nm and 2.5 nm as dielectric as shown in Figure 3.19(a). It was previously reported that it is possible to tune the defect concentration in $\mathrm{GaO_x}$ layer by modifying the deposition parameters [202]. As per this study, the ALD $\mathrm{GaO_x}$ films deposited with oxygen plasma times of few seconds (3-8 s) have significant concentration of defect levels (which we assume can act as charge traps). The switching I-V, P-V and PUND sequence P-V measurement corresponding to 3 nm $\mathrm{GaO_x}$ are shown in Figure 3.19(b), (c) and (d). The same for 2.5 nm $\mathrm{GaO_x}$ are shown

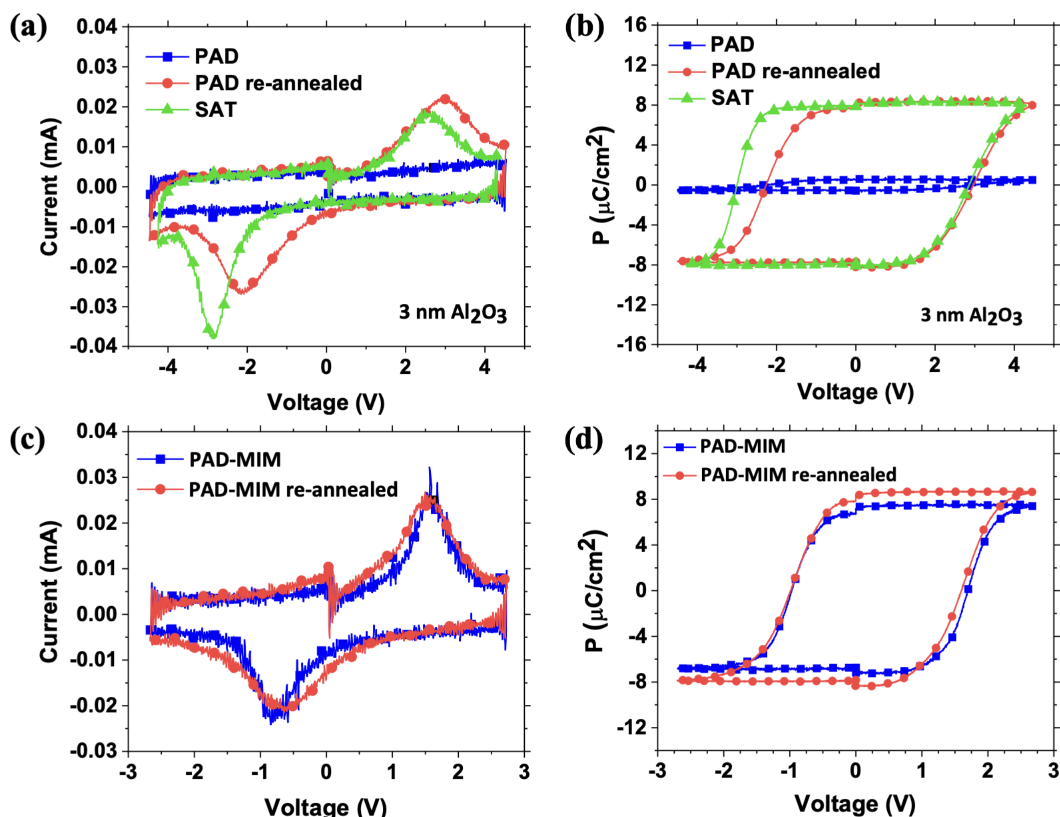

Figure 3.18: (a) Switching I-V and (b) PUND sequence P-V measurement corresponding to 2000 cycles for PAD device with Al_2O_3 thickness of 3 nm before and after the RTP re-annealing of 400 °C, 120s in N_2 atmosphere. The switching I-V and PUND sequence P-V measurement for SAT device after 2000 cycles are also shown in (a) and (b). (c) Switching I-V and (d) PUND sequence P-V measurement at 2000 cycles for PAD-MIM stack before and after the RTP re-annealing. The polarization switching measurements and wake-up cycling for SAT, PAD and PAD-MIM stacks are performed the same way as discussed in Figure 3.13 and Figure 3.14 respectively.

in Figure 3.19(e), (f) and (g). The GaO_x films were grown using 1 s O_2 plasma time. The PAD stack with both 3 nm and 2.5 nm GaO_x layer show a small P_R of $\sim$ 1.5 $\mu C/cm^2$ in the pristine state and after wake-up of 2000 cycles, the P_R increases to $\sim$6 $\mu C/cm^2$ for 3 nm and $\sim$7.5 $\mu C/cm^2$ for 2.5 nm of GaO_x layer. This supports our hypothesis and shows that if there are sufficient charge traps in the dielectric, the stack shows polarization switching. Therefore, it also shows a possible approach to engineer charge trap density in the dielectric layer and the performance of FTJ stack.

In the PAD stack with thick ferroelectric layer of $\sim$3 nm thickness, if we are able to provide carriers to the HZO-Al_2O_3 interface, we might be able to stabilize the polarization and observe ferroelectric switching. It was shown with GaO_x layer that it is indeed

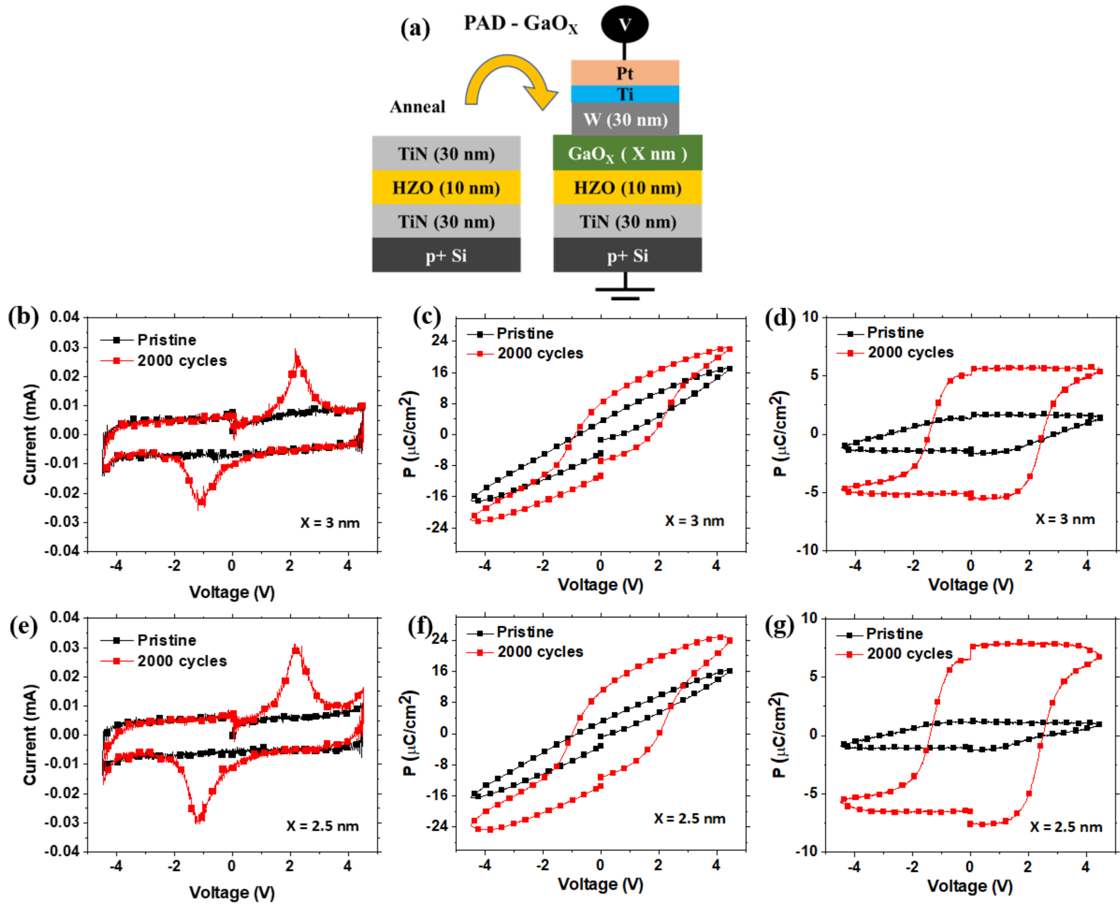

Figure 3.19: (a) Schematic representation of post anneal deposition (PAD-GaO_x) stack with GaO_x thickness as X nm. Here the HZO crystallization is performed on TiN-HZO-TiN stack and then the top TiN is removed and GaO_x layer and W top electrode are deposited and patterned through Ti/Pt lift off followed by W etching. (b) Switching I-V, (C) P-V and (d) PUND sequence P-V measurements corresponding to pristine and 2000 cycles for PAD device with GaO_x thickness of 3.0 nm. (e) Switching I-V, (f) P-V and (g) PUND P-V measurements corresponding to pristine and 2000 cycles for PAD device with GaO_x thickness of 2 nm. For both the stacks, polarization switching is carried out with triangular pulse of $\pm$ 4.5 V, 1ms and wake-up cycling is performed with triangular pulse of $\pm$ 4.5 V and 1kHz frequency. Oxygen plasma time of 1 s is used for GaO_x deposition in both stacks.

possible. However, the charge trap concentration in dielectric layers is usually limited to low values (10^{12}-10^{14} /cm^2). A metal on the other hand has very high carrier concentration. So, a new stack was fabricated named 'PAD-2 nm TiN' using a ultra-thin TiN layer as shown in Figure 3.20(a). Similar to the PAD stack, here as well we first crystallize the HZO in TiN-HZO-TiN architecture. Then the top TiN is etched away and a TiN layer of $\sim$2 nm is deposited. After that a 3 nm Al_2O_3 layer and W top electrodes are deposited and patterned. As there is a blanket TiN layer between the HZO and Al_2O_3, RIE etching

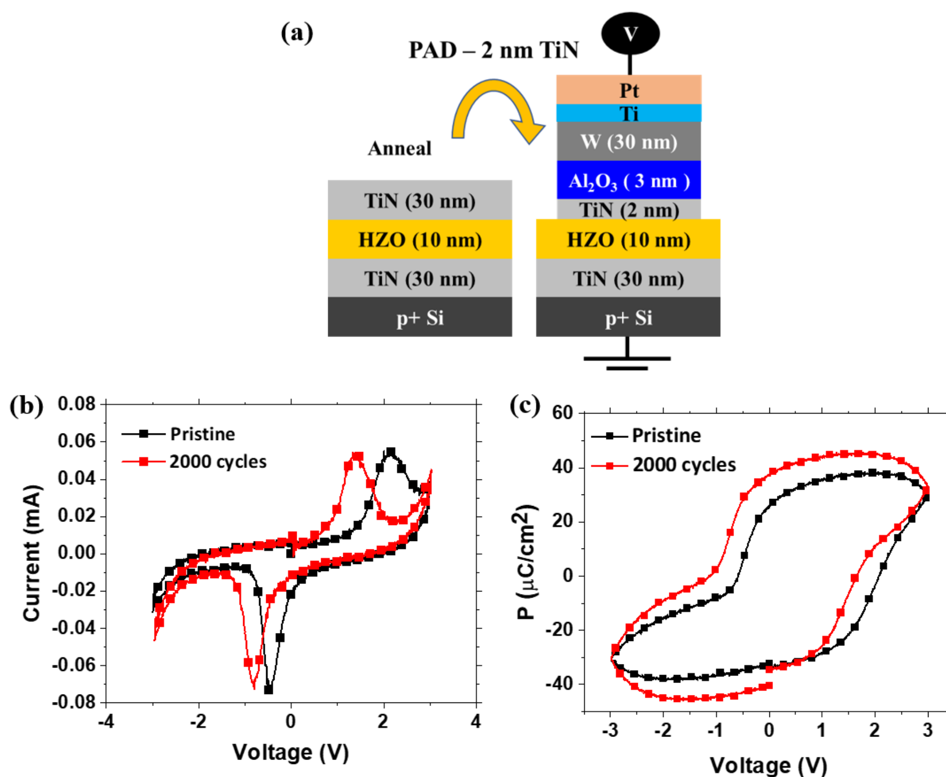

Figure 3.20: (a) Schematic representation of post anneal deposition device with 2 nm TiN between HZO and Al_2O_3 layer (PAD-2 nm TiN). The switching (b) I-V and (b) P-V measurement corresponding to PAD- 2nm TiN at pristine and 2000 cycles. Here the wake-up cycling is performed with 3.0 V, 1 kHz triangular waveform and the polarization switching measurements are performed with triangular waveform of 3.0 V and 1 ms.

with SF_6 is used to remove it outside the device area. The 2 nm thick TiN is assumed to help in stabilizing the polarization through charge compensation. The switching I-V and P-V measurements corresponding to the stack are shown in Figure 3.20(b) and (c). Even though the dielectric layer is 3 nm Al_2O_3, the stack shows polarization switching from the pristine state onwards. The free carriers in the 2 nm TiN metal help in the compensation of polarization.

In case of SAT and PAD stacks, the dielectric is placed near the top electrode. Now, two FTJ stacks are fabricated with different process flows to get FTJ devices, where the dielectric was placed near the bottom electrode as shown in Figure 3.21. It was observed that placing the dielectric near the bottom electrode is more favorable than placing the dielectric near the top electrode (discussed in Section 3.2). The first stack is called stack anneal bottom (SAB), shown in Figure 3.21(a). Here the annealing was done on the entire M-FE-DE-M stack with TiN bottom electrode and W top electrode. The second stack is

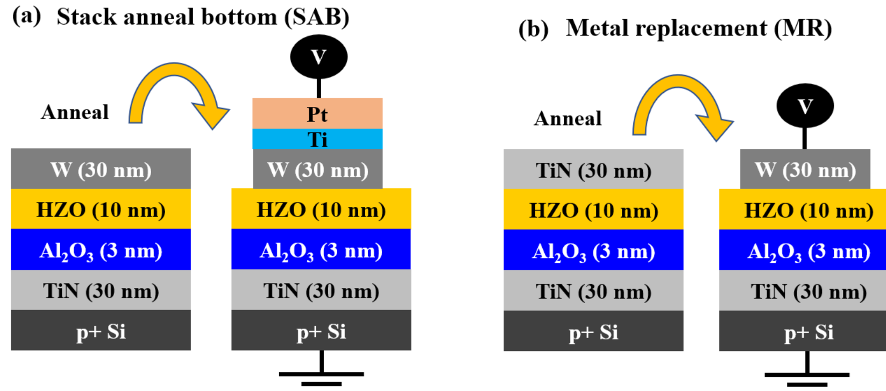

Figure 3.21: (a) Schematic representation of stack anneal bottom (SAB) device with Al_2O_3 placed near bottom electrode. Here the HZO crystallization annealing is done on the M-FE-DE-M stack with TiN bottom electrode and W top electrode and then the top electrode is patterned by Ti(10nm)/Pt(100nm) lift off and W wet etch. (b) Schematic representation of metal replacement (MR) device. Here the HZO is crystallized by annealing M-FE-DE-M stack with TiN as bottom and top electrodes. Then the TiN top electrode is removed by wet etching and W top electrode is lifted off. For both the stacks, HZO crystallization is done with RTP of 400 °C, 120 s in N_2 atmosphere.

called metal replacement (MR), shown in Figure 3.21(b). Here the HZO crystallization annealing is first done on the TiN-Al_2O_3-HZO-TiN stack. After the annealing, TiN top electrode was etched with SC1 solution at 50 °C and 30 nm W electrode was patterned as the new top electrode metal with lift-off process. So, the difference between the two stacks are that in SAB stack, the crystallization annealing was done with W top electrode and in case of MR stack, the crystallization anneal was carried out with TiN top electrode and it was replaced with W post-anneal.

The switching I-V, P-V and PUND sequence P-V measurements corresponding to SAB stack is shown in Figure 3.22(a), (b) and (c) respectively. The electrical pulse conditions used for measurements and cycling are mentioned in the figure caption. The stack shows switching behavior from pristine state and the P_R value after 2000 cycle is ~ 9 $\mu C/cm^2$ (in the positive polarity). The switching I-V, P-V and PUND sequence P-V measurement corresponding to MR stack are shown in Figure 3.22(d), (e) and (f) respectively. From the I-V measurement, we can see that the MR stack shows more leakage current in the positive polarity and the stack shows P_R value of ~ 10.5 $\mu C/cm^2$ (in the positive polarity) after wake-up. Here we can see that even though the final stack architecture for both stacks are similar, the switching characteristics are different. The read measurements, ON/OFF ratio and the ON-OFF current corresponding to SAB and MR

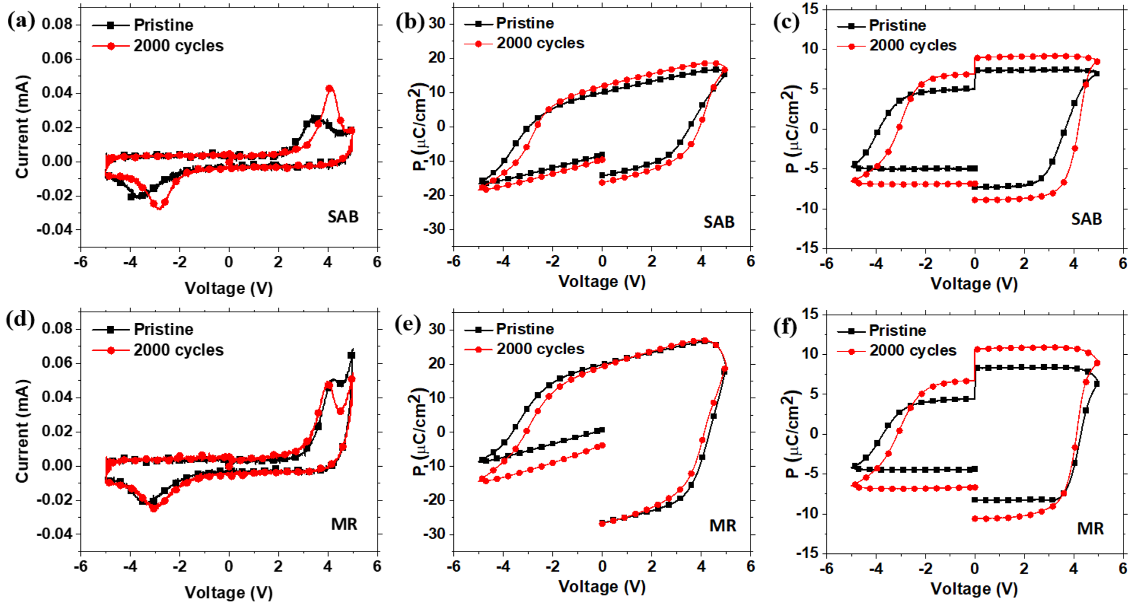

Figure 3.22: (a) Switching I-V, (b) P-V and (c) PUND sequence P-V measurements corresponding to pristine and wake-up state of 2000 cycles for SAB device. Here the polarization is switched with triangular pulse of ±5.0 V, 1 ms and the wake-up cycling is performed with triangular waveform of ±5.0 V and 100 Hz frequency. (d) Switching I-V, (e) P-V and (f) PUND sequence P-V measurements corresponding to pristine and wake-up state of 2000 cycles for MR device. Here the polarization is switched with triangular pulse of ± 5.0 V, 1 ms and the wake-up cycling is performed with triangular waveform of ±5.0 V and 100 Hz frequency.

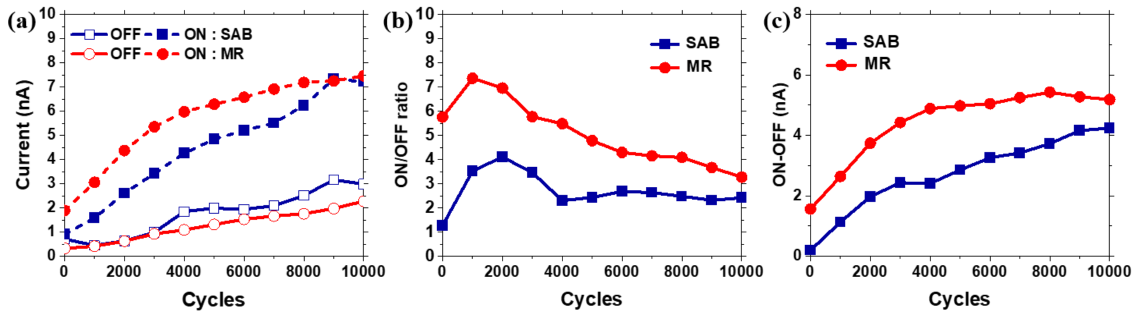

Figure 3.23: (a) Evolution ON and OFF currents from pristine to 10^4 cycles for stack SAB and MR. (b) Evolution of ON/OFF ratio from pristine to 10^4 cycles (c) Evolution of ON and OFF current difference from pristine to 10^4 cycles. For both the stacks, reset operation is performed with triangular monopolar pulse of -5.0 V, 0.5 ms and Set operation is performed with triangular monopolar pulse of +5.0 V, 0.5 ms. Read operation is performed by applying DC voltage of +2.0 V.

devices are shown in Figure 3.23(a), (b) and (c) respectively. The higher remnant polarization of MR stack translates to higher ON current and lower OFF current, leading to high ON/OFF ratio. The MR stack also shows higher ON-OFF current difference. The reason for the difference in their behavior is not clear. It is likely that different charge

trap concentration and interfaces resulting from difference in the process flows lead to the observed characteristics.

3.7 Quantification of charge traps in the FTJ stack

From the previous section, we suggest that charge traps have a crucial role in the functioning of bilayer FTJ devices. In the SAB stack, when the HZO crystallization annealing was performed in the presence of Al_2O_3 dielectric, the stack shows a high P_R value after wake-up. In the PAD stack, when the crystallization annealing was done on TiN-HZO-TiN stack, the FTJ stack did not show polarization switching even after undergoing wake-up cycling even though this stack also has the same M-FE-DE-M device architecture. This qualitatively showed us that in SAB stack there are more charge traps compared to PAD stack. In-order to quantify the effect of charge traps in the SAB and PAD stacks, device simulations were performed by the group of Dr. Esseni (Polytechnic Department of Engineering and Architecture (DPIA) at the University of Udine). They have used their in-house numerical model to fit our experimental data [203–205]. This work has been published as Fontanini et al [206].

In the simulation, the FE domain dynamics is solved through multi-domain Landau-Ginzburg -Devonshire (LGD) equations accounting 3D electro-statistics. The free parameters in the model are the LGD constants (α_i, β_i, γ_i), resistivity of the FE domains (ρ) which sets the time scale for FE switching and the domain wall coupling constant (k). ρ is taken as 100 Ωm and k $\approx$ 0. This is consistent with the recent reports based on HZO capacitor structures [207–209]. Even though additional effects are also possible, the read current is assumed to be dominated by tunneling across the dielectric layer. In the model, the charges due to charge injection and trapping are represented as effective areal densities at the FE-DE interface. It is possible that the actual location of the charge trap is within the FE or DE films. The trap occupation (f_T) is solved through first-order dynamic equations for each energy level (E_T) at the FE-DE surface by assuming Fermi occupation function in the metal electrode near ferroelectric (M_F) and the metal electrode near the dielectric (M_D). In these simulations, Q_{acc} and Q_{don} are the acceptor and donor traps. They depend on f_T and are proportional to the acceptor (N_{acc}) and donor (N_{don}) trap densities. The work functions of W and TiN electrodes are taken as 4.5 eV. The tunneling

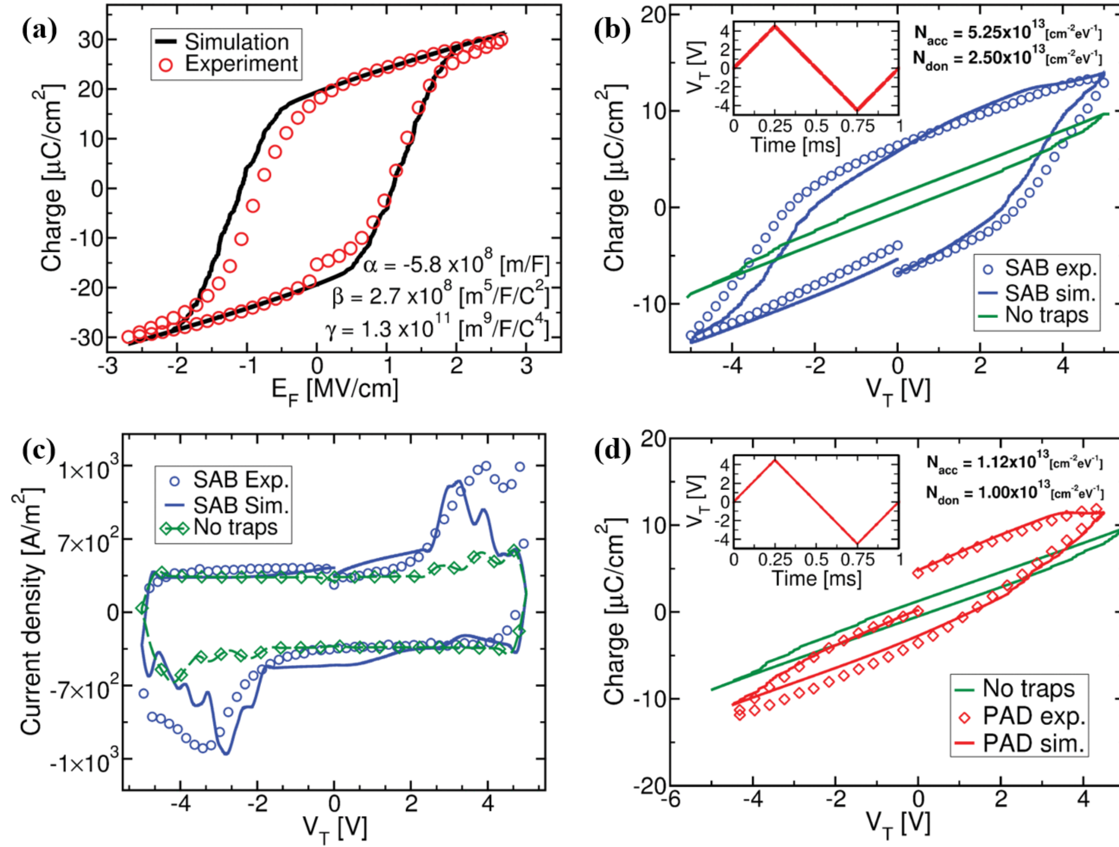

Figure 3.24: (a) Comparison of experimental data and simulation of charge versus electric field for TiN(30nm)-HZO(10nm)-TiN(30nm) device. The mean values of the LGD constants are mentioned as insets. (b) Comparison of experimental data and simulation of charge versus switching voltage on SAB device with 3 nm Al_2O_3.The simulation with no charge traps are shown with green line and simulation accounting acceptor and donor traps are shown with blue line. (c) Switching I-V curve corresponding to the SAB stack and the simulated switching curve is shown here. The trap densities used for simulation in (b) and (c) are same and are as follows N_{acc} =5.25$\times$10^{13} cm^{-2}eV^{-1} and N_{don} = 2.5$\times$10^{13} cm^{-2}eV^{-1}. (d) Comparison of experimental data and simulation of charge versus switching voltage on PAD device with 3 nm Al_2O_3. The simulation with no charge traps are shown with green line and simulation accounting acceptor and donor traps are shown with red line which fits very well with the experimental data. The trap densities used for the simulation here as N_{acc} = 1.12$\times$10^{13} cm^{-2}eV^{-1} and N_{don} = 1.0$\times$10^{13} cm^{-2}eV^{-1}. The experimental data corresponding to (a)-(d) are after a wake-up of 2000 cycles and the polarization switching is measured using triangular waveform showed as inset in (b) and (d). Figures are reproduced from Fontanini et al [206] (© [2022] IEEE).

mass (m) and permittivity (ϵ) are assumed to be m_{FE} = 0.38 m_0, ϵ_{FE} = 34 ϵ_0 for HZO and m_{DE} = 0.15 m_0, ϵ_{DE} = 10 ϵ_0 for the Al_2O_3 layer. Here m_0 is the free electron mass and ϵ_0 is the permittivity of vacuum.

The model is calibrated by fitting the simulation to the experimental data of charge versus electric field measurements on a TiN-HZO-TiN stack as shown in Figure 3.24(a). The simulation fits very well with the experimental data except the slight asymmetry in the measured P-V data. This can be due to the difference between the TiN-HZO interface at the bottom and the top. From the calibration, the LGD constants are extracted to be $\alpha = -5.8 \times 10^8 \mathrm{m/F}$, $\beta = 2.7 \times 10^8 \mathrm{m^5/F/C^2}$ and $\gamma = 1.3 \times 10^{11} \mathrm{m^9/F/C^4}$. In Figure 3.24(b) and (c) it is evident that in the absence of charge traps, the switching characteristics are not present in the P-V or I-V switching curves. A good fitting is only achieved by incorporating adequate $\mathrm{N_{acc}}$ and $\mathrm{N_{don}}$ charge densities at the FE-DE interface. In the SAB device, after wake-up of 2000 cycles, the charge trap densities are estimated to be $\mathrm{N_{acc}} = 5.25 \times 10^{13} \mathrm{cm^{-2}eV^{-1}}$ and $\mathrm{N_{don}} = 2.5 \times 10^{13} \mathrm{cm^{-2}eV^{-1}}$ (shown in Table 3.1). The same analysis is performed on the PAD device with the polarization switching P-V measurement at 2000 cycles as shown in Figure 3.24(d). The simulation shows large discrepancy with the measurement data, when the charge traps are not accounted in it. By incorporating charge traps in the simulation, a good fit to the experimental data is achieved for charge trap densities of $\mathrm{N_{acc}} = 1.12 \times 10^{13} \mathrm{cm^{-2}eV^{-1}}$ and $\mathrm{N_{don}} = 1 \times 10^{13} \mathrm{cm^{-2}eV^{-1}}$. This charge trap densities are significantly smaller than that we estimated in the SAB device. Since both the stacks underwent similar wake-up conditions, the difference in the amount of charge traps are possibly arising from the difference in the annealing conditions for the two devices. This further confirms our hypothesis that it is indeed the amount of charge traps that leads to the difference in the switching behavior of the two stacks.

Stack	$\mathrm{N_{acc}}$ $\mathrm{cm^{-2}eV^{-1}}$	$\mathrm{N_{don}}$ $\mathrm{cm^{-2}eV^{-1}}$
SAB	5.25×10^{13}	2.5×10^{13}
PAD	1.12×10^{13}	1.0×10^{13}

Table 3.1: Estimated charge trap densities in SAB and PAD stacks.

3.8 Confirmation of charge traps through C-V and polarization measurements

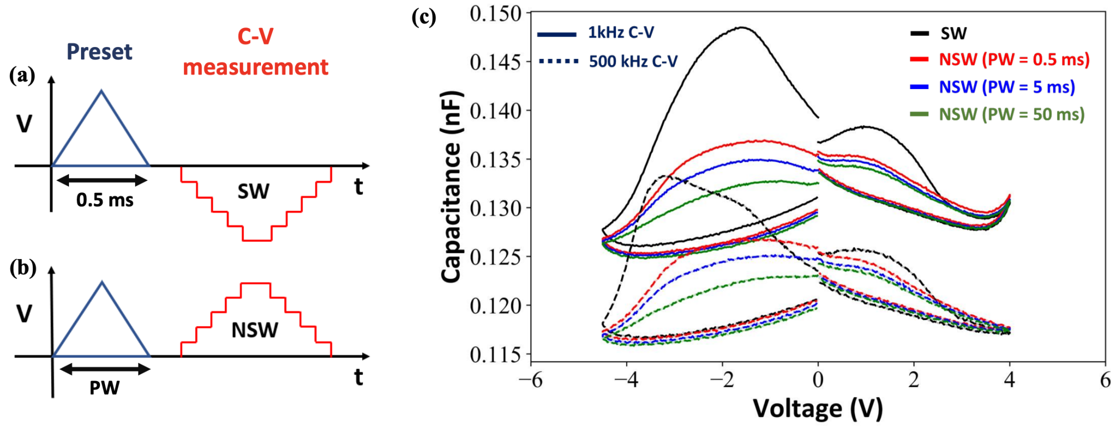

Figure 3.25: (a) Measurement sequence for switching (SW) C-V measurement. A triangular preset pulse of 0.5 ms pulse width is followed by a quasi-static C-V measurement of opposite polarity. (b) Measurement sequence for non-switching (NSW) C-V measurement. A triangular preset pulse of 'PW' pulse width is followed by a quasi-static C-V measurement of same polarity. NSW measurement is taken for PW values of 0.5 ms, 5 ms and 50 ms. (c) C-V measurement corresponding to SW and NSW sequences. The same measurements are performed in 1 kHz frequency (solid lines) and 500 kHz frequency (dashed lines). These measurements are performed on SAB device after wake-up of 2000 cycles.

In-order to estimate the charge trap densities experimentally, we performed quasi-static C-V measurements on SAB device as shown in Figure 3.25. The C-V measurements are performed with different preset pulses to set the polarization state prior to the measurement. The C-V measurements performed after a triangular preset pulse of opposite polarity as that of the C-V measurement is called switching (SW) measurement and is shown in Figure 3.25(a). Here the preset operation switches the entire polarization to one direction and the SW measurement switches all the domains to the opposite direction. Thus, this C-V measurement consists of switching dynamics from majority of the domains. This is shown as black curves in Figure 3.25(c). The solid black line represents the C-V measurement at 1 kHz frequency and the dashed line represents the C-V measurement at 500 kHz frequency. The C-V measurement taken after the preset of same polarity is known as the non-switching (NSW) measurement. NSW measurement is taken with different preset pulse widths. From Figure 3.25(c) we can see that with the increase

in NSW preset pulse width from 0.5 ms to 50 ms, the corresponding C-V measurement peak decreases. A typical small signal C-V measurement on ferroelectric layers has a hysteretic loop (often called 'butterfly curves'). The measurements where the DC sweep switches the polarization during the C-V measurement shows a peak in capacitance due to varying dielectric constant during switching. The magnitude of capacitance is considered proportional to the domain number in the ferroelectric. Therefore, it has a peak around the coercive voltage where the number of domains is the highest. In the measurements in Figure 3.25(c) it is clear that with increase in the preset pulse width, more domains are getting switched during the preset operation and that leaves fewer domains for the C-V measurement to switch. Since the charge trap charging/discharging has a longer time scale than the polarization switching, this effect directly indicates the presence of charge traps in this stack.

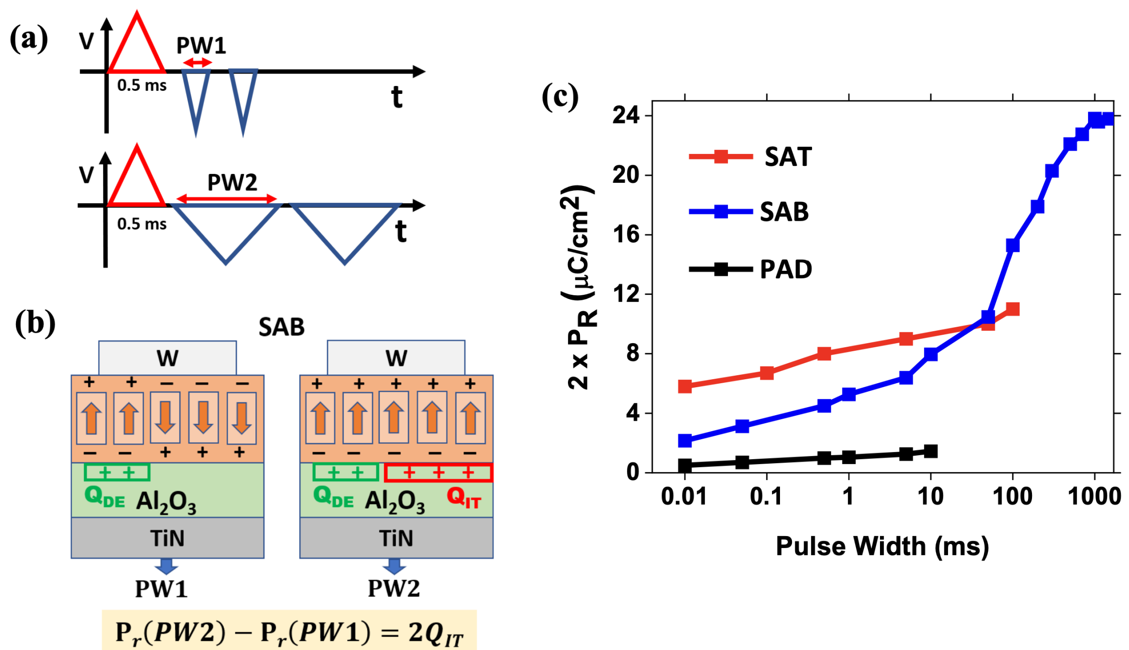

Figure 3.26: (a) Schematic showing custom P_R measurement technique. A triangular set pulse of 0.5 ms is applied on the device followed by two triangular reset pulses. This measurement is repeated for different reset pulse widths varying from the lowest value, PW1 to the highest value PW2. (b) Schematic representation of how lower reset pulse width leads to small remnant polarization due to the inability to charge/discharge trap densities and how larger reset pulse width leads to increased remnant polarization. As the reason for higher remnant polarization is the charging or discharging of traps, this can be used to estimate the charge traps as shown in (b). (c) Polarization versus reset pulse width measurement result corresponding to SAT, SAB and PAD stacks. These measurements are performed on the devices after wake-up of 2000 cycles.

From the pulse dependent NSW C-V measurement it is clear that more domains are switching when the pulse width of the switching preset pulse is increased. To estimate the amount of charges switching during each pulse width, a custom polarization measurement technique is used. This method is inspired from the PUND sequence P-V measurement. Here the polarization of the device is switched to the set state with a triangular voltage pulse of corresponding amplitude and 0.5 ms pulse width. Then two triangular voltage pulse of opposite polarity (reset pulse) are applied one after the other and the charge from the device is measured during each pulse. The charge from the first reset pulse contains charge from polarization switching as well as from the linear, non-linear capacitance, leakage, etc. Whereas in the second reset pulse, all other components remain same except the remnant polarization switching. So, by subtracting the charge corresponding to the second reset pulse from the first reset pulse we get the remnant polarization ($2P_R$) of the device. But it needs to be mentioned that this will be in the ideal case where all the domains switch in the first reset pulse itself. We know from SW C-V measurements that this is not the case. Depending on the pulse width of the first reset pulse, the number of domains switching can be different. It mainly depends on the quantity of charge traps that are getting charged/discharged during that reset pulse and resulting stabilized polarization. Therefore, the second reset pulse might also lead to some polarization switching. However, the quantity of switched polarization in the second reset pulse can be assumed to be lower than in the first one. Thus, the technique is still valid and helps us to quantify the amount of remnant polarization achieved with different pulse widths of the reset pulse. The value we measure may be slightly lower than the actual switched polarization.

The pulse sequence used for the custom P_R measurement is shown in Figure 3.26(a). The preset is done with a set pulse and the $2P_R$ is measured by applying two reset pulses and by calculating the difference in charge corresponding to the two reset pulses. The measurement is repeated for different reset pulse widths. The lowest pulse width used is marked as PW1 and the highest pulse width used is marked as PW2. In Figure 3.26(c), we can see that, with the increase in pulse width used for the reset pulse, the P_R increases. This is because when we apply a large pulse width, it is possible for the charge traps to get charged/discharged due to its larger time scale which ultimately helps in the stabilization of polarization. The same measurement is performed on SAT, SAB and PAD devices.

SAT and PAD devices do not survive measurements with large reset pulse widths. The charge traps are estimated on these devices by using the relation showed in Figure 3.26(b). The charge traps in FE-DE stack needed to stabilize remnant polarization of $\sim 12\mu\mathrm{C/cm^2}$ are found to be $\sim 10\mu\mathrm{C/cm^2}$. Such a high charge density needed indicates that interface traps are central to FTJ device design.

3.9 Summary

In this chapter we discussed various aspects affecting the performance of bilayer FTJ stacks with TiN, W metal electrodes, HZO ferroelectric layer and $\mathrm{Al_2O_3}$ dielectric. We showed that the placement of dielectric layer as well as the positioning of metal electrodes plays an important role in attaining high performance FTJ devices. We found that W bottom electrode provides optimum performance in terms of ON/OFF ratio for the bilayer FTJ stack with W and TiN electrodes. It was also found that placing $\mathrm{Al_2O_3}$ next to bottom electrode also contributes to better FTJ performance. We also demonstrated that the charge traps in the dielectric (or at DE-FE interface) play an important role in the switching behavior of FE in M-FE-DE-M FTJ stack and higher concentration of charge traps leads to stabilization of larger polarization in the FE layer. The fabrication process flow directly impacts the charge trap densities resulting in different switching behaviors. Here we showed that annealing the DE-FE interface generates charge traps (possibly also changing the oxygen vacancy concentration). We further demonstrated that a longer pulse is needed to stabilize higher remnant polarization, which may be associated with the time required to charging/discharging of the charge traps and to the movement of ions that also contribute to trap density or charge compensation. This could limit the attainable ON/OFF ratio with shorter pulse width. With the help of simulation, the donor and acceptor charge densities were estimated in the FE-DE interface for stacks with different process sequence. A difference in the amount of charge traps leads to the difference in $\mathrm{P_R}$ and thus in the difference of ON current and ON/OFF ratios.

Chapter 4

Impact of electrical parameters on the device performance

4.1 Introduction

The phenomenon commonly named to as ”wake-up” behavior refers to the emergence of a notably high remnant polarization in ferroelectric HZO layer following electric field cycling. Numerous hypotheses attempt to explain wake-up behavior, attributing it to oxygen vacancy redistribution [210,211], phase transformation during field cycling [181,212], or electron trapping [213]. The wake-up phenomenon in M-FE-M capacitor structures has been previously studied [213–217]. However, regarding FTJs, there has been a limited exploration of the impact of electrical field cycling parameters on the FTJ device behavior. Understanding how the electrical waveform parameters influence the device characteristics is critically important in the context of FTJ memory and synaptic devices, to gain insight into the wake-up mechanism in FTJs and to design appropriate circuits for enabling efficient wake-up.

Only recently has a study explored the impact of cycling scheme within TiN-Al_2O_3-HZO-TiN bilayer FTJ devices [218]. The complexity of circuits required to initiate wake-up in the FTJ stack depends on the specific waveform needed. Moreover, in the context of neuromorphic applications, the attainable number of resistance states depends greatly on the ON/OFF ratio and ON-OFF current difference of the FTJ, which is closely tied to the wake-up polarization resulting from the electrical cycling. Additionally, the stability

of the polarization state in bilayer devices is affected by charge traps near the FE-DE interface as discussed in Section 3.7 of Chapter 3 [206]. The role of these charge traps during wake-up has not been previously studied in bilayer FTJ stacks.

Once the ferroelectric layer is woken up, different pulse schemes can be used to switch the domains gradually, in order to attain multiple resistance states through partial switching operations. This ability to finely manipulate resistance levels of the device is a crucial aspect in the context of neuromorphic computing and non-volatile memory applications [121]. By modulating the net remnant polarization of the ferroelectric material through controlled pulse sequence, it becomes feasible to emulate synaptic behavior in FTJ based electronic circuits. This emulation of synaptic plasticity in FTJ devices can be utilized for the development of energy-efficient brain-inspired computing systems, where the device can store and process information in a manner akin to the human brain's neural connections.

In this chapter, we investigate the impact of electrical parameters on the wake-up behavior and partial switching operation on TiN-Al_2O_3-HZO-W FTJ devices. These stacks were discussed in Chapter 3 as stack C. We investigate how different cycling waveforms influence the polarization of the HZO layer within the stack and their subsequent impact on the ON/OFF ratio. Our findings reveal that the wake-up behavior and memory characteristics are significantly influenced by the specific waveform employed during the field cycling operation.

The discussion in this chapter is published in paper titled "Cycling waveform dependent wake-up and ON/OFF ratio in Al_2O_3/$Hf_{0.5}Zr_{0.5}O_2$ ferroelectric tunnel junction devices" in the journal of ACS Applied Electronic Materials [219], made available under a Creative Commons Attribution Licence (CC BY 4.0).

4.2 Cycling waveform dependent wake-up and ON/OFF ratio

We initially examined the wake-up behavior in TiN-Al_2O_3-$Hf_{0.5}Zr_{0.5}O_2$-W FTJ devices using four distinct field cycling waveforms, triangular and square waveforms at frequencies of 1 kHz and 100 Hz. The frequency range holds particular significance in the context

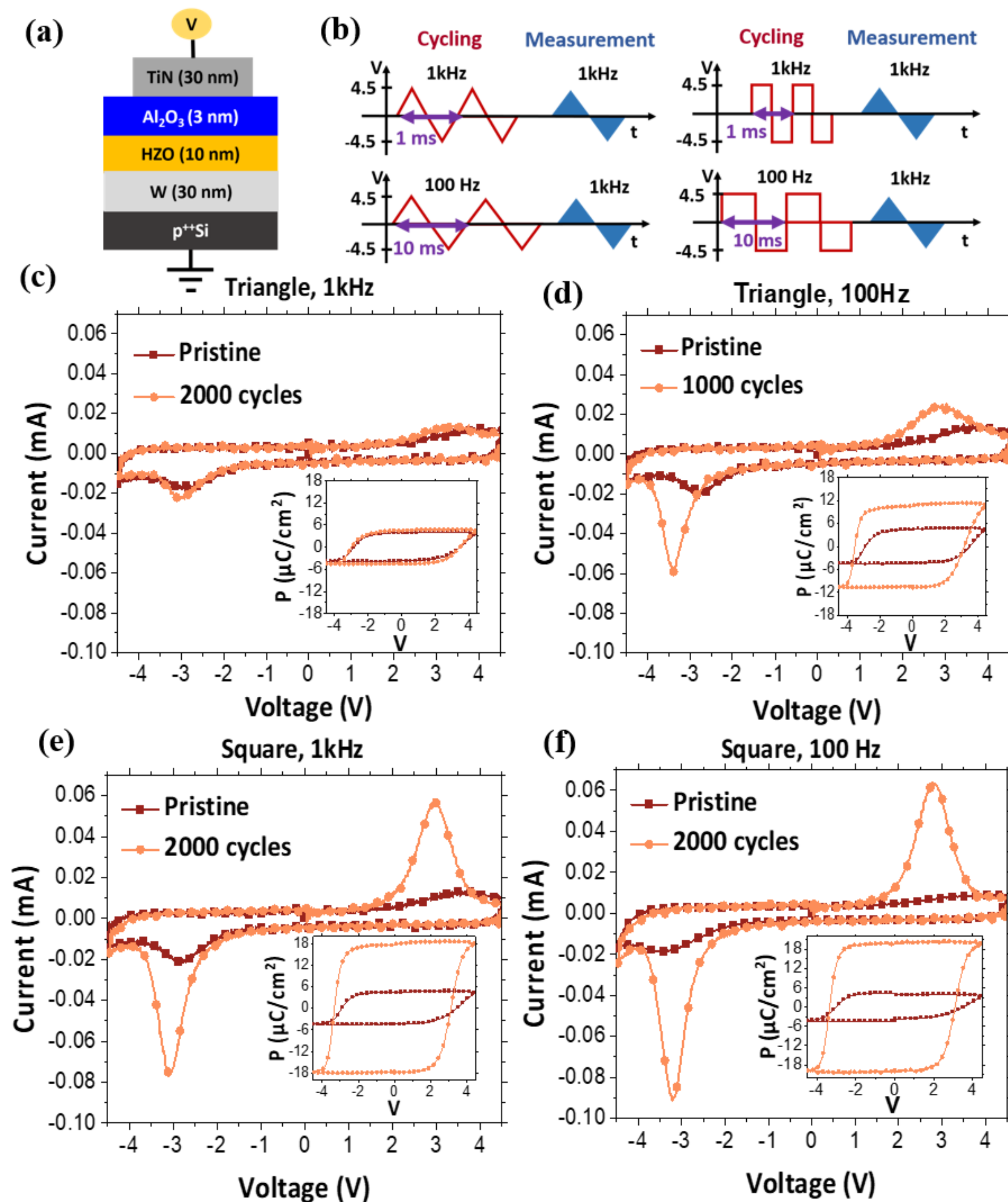

Figure 4.1: (a) Schematic illustrating the TiN-Al_2O_3-$Hf_{0.5}Zr_{0.5}O_2$-W FTJ stack and measurement configuration. (b) The wake-up field cycling and measurement sequence correspond to four distinct cycling waveforms: 1 kHz, 100 Hz triangular, and 1 kHz, 100 Hz square. Following field cycling, I-V and P-V measurements are conducted using a triangular waveform with a frequency of 1 kHz and a voltage range of ±4.5 V. (c) and (d) display I-V measurements for the 1 kHz, 100 Hz triangular waveform, while (e) and (f) showcase I-V measurements for the 1 kHz, 100 Hz square waveform. Each curve depicts the pristine state as well as the post-wake-up cycles. The insets in (c)-(f) present the PUND sequence P-V measurements. Figures are reproduced from Nair et al [219].

of FTJ-based neuromorphic circuits operating on biological time scales [138, 220], with device switching expected to occur at frequencies on the order of several hundred hertz. Therefore, we conducted the wake-up study at two frequencies, 1 kHz and 100 Hz. The results of the measurement are presented in Figure 4.1. All the applied waveforms have a voltage amplitude of ±4.5 V, as illustrated in Figure 4.1(b). The I-V and PUND P-V measurements, both before and after the wake-up cycles using these waveforms, are depicted in Figure 4.1(c)-(f). In all the measurements, the wake-up state is considered after 2000 cycles, as our TiN-HZO-TiN capacitors typically require 2000 cycles of wake-up cycling using a 1 kHz triangular waveform [221], discussed in Section 2.6 of Chapter 2. In our measurement setup, square pulses with amplitudes up to 5.0 V can be consistently applied without distortion for frequencies up to 1 kHz.

All measurements were conducted using bipolar triangular pulses with a width of 1 ms, featuring a voltage sweep sequence of 0 $\rightarrow$ +4.5 V $\rightarrow$ 0 $\rightarrow$ -4.5 V $\rightarrow$ 0, as depicted in Figure 4.1(b). In the pristine state, a modest $\mathrm{P_R}$ of 4-5 $\mu\mathrm{C/cm^2}$ is observed. The P-V loops exhibit no pinching, providing clear evidence of ferroelectric behavior. Notably, in the I-V measurements, the peak of the switching current is broader in positive polarity as compared to negative polarity. In positive polarity it extends above 4.0 V, whereas in negative a minimum is observed around -4.0 V. In P-V measurements, this manifests as a reduced slope of the curve during the transition from -$\mathrm{P_R}$ to +$\mathrm{P_R}$ and a steeper curve during the reverse transition from +$\mathrm{P_R}$ to -$\mathrm{P_R}$. This phenomenon signifies a broad range of coercive voltages, with certain domains remaining unswitched during the positive polarity voltage sweep, potentially having coercive voltages surpassing 4.5 V. The asymmetry in the coercive voltage distribution for both polarities is more pronounced compared to a standard M-HZO-M stack. This variation can be attributed to the presence of the dielectric-ferroelectric interface on one side, where domain pinning may arise due to the presence of charge traps or oxygen vacancies, especially for domains with polarization directed towards $\mathrm{Al_2O_3}$ layer. A similar domain pinning phenomenon has been documented in TiN-HZO-TiN stacks when the bottom TiN electrode had undergone oxide formation [222]. Therefore, the $\mathrm{Al_2O_3}$-HZO interface charge configuration can lead to certain domains having notably high coercive voltages, exceeding the 4.5 V as observed in the devices.

As seen in Figure 4.1(c), the wake-up effect following a cycling with 1 kHz triangular waveform appears to be relatively weak, marked only by a slight increase in the switching current peak and a corresponding low magnitude of the remnant polarization. Over 2000 cycles, the coercive voltage distribution of domains shows minimal alteration from its pristine state. When wake-up cycling is conducted using a 100 Hz triangular waveform a substantial increase in the switching current peak becomes evident after 1000 cycles (Figure 4.1(d)). The magnitude of the $2\mathrm{P_R}$ increases to ~20 $\mu\mathrm{C/cm^2}$. The coercive voltage for the positive polarity diminishes, and the range of coercive voltages exhibited by domains becomes narrower compared to their pristine state. An even more pronounced enhancement in wake-up effect is evidenced when employing a square waveform at a frequency of 1 kHz, as depicted in Figure 4.1(e), and this further improves at 100 Hz (Figure 4.1(f)). The increase in remnant polarization when utilizing square waveforms significantly surpasses that observed with the two triangular waveforms, resulting in remarkably high $2\mathrm{P_R}$ of ~35 $\mu\mathrm{C/cm^2}$ at 1 kHz and about 39.5 $\mu\mathrm{C/cm^2}$ at 100 Hz. In both square waveforms, the coercive voltage distribution in positive polarity after wake up, as indicated by the width of the switching current peak, is substantially diminished when compared to the two triangular waveforms. This observation implies that a significantly larger proportion of domains are now undergoing switching, as the coercive voltage for most domains falls well below the maximum applied voltage (the switching current peak is achieved at ~3.0 V). This increased number of domains that are now switching are the domains that initially had high coercive voltages (exceeding 4.0 V in the pristine state). For the reason of this effect, we propose that these domains have undergone depinning during cycling with the square waveform, resulting in a reduction of their coercive voltage during subsequent wake-up cycles [213, 217].

In order to further probe the impact of voltage amplitude, we perform wake-up with various voltage amplitudes starting with ±3.0 V and up to ±5.0 V. Cycling operation performed with the lowest voltage amplitude of ±3.0 V is shown in Figure 4.2. It shows that $\mathrm{P_R}$ decreases with cycling. Here rather than wake-up, less and less domains switch with cycling. Based on the coercive voltage distribution observed in pristine state in Figure 4.1, this amplitude is clearly insufficient to switch a majority of the domains, particularly in positive polarity, which possibly results from the pining of many domains

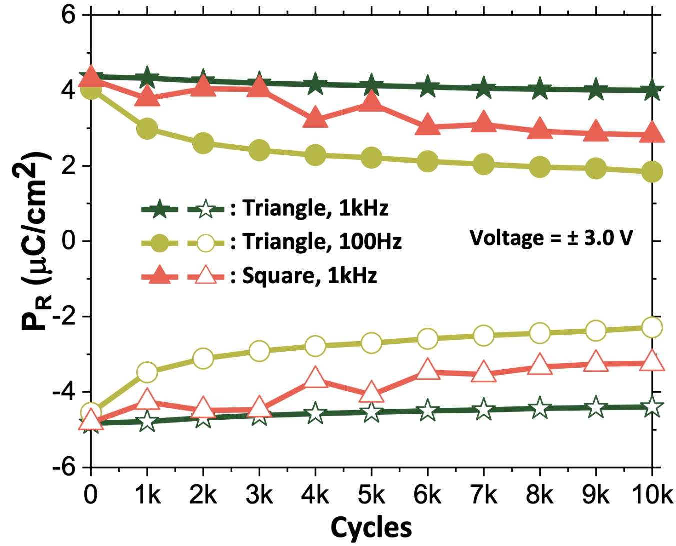

Figure 4.2: The evolution of remnant polarization from its pristine state to 10^4 cycles under cycling conditions featuring triangular waveforms at both 1kHz and 100Hz frequencies, as well as square waveforms at 1kHz frequency, all with a pulse amplitude of 3V. Here, the PUND P-V measurements are performed using a triangular waveform with frequency 1 kHz and voltage amplitude of ±4.5 V.

[217]. In Figure 4.3(a)-(d), we show the wake-up behavior for voltage amplitudes of 4.0, 4.5, and 5.0 V. We plot the dependence of remnant polarization from its pristine state to 10^4 cycles for the four distinct wake-up waveforms. It becomes evident that achieving wake-up is not attainable when cycling is performed at 4.0 V for all waveforms and frequencies, with the exception of the 100 Hz square waveform. Despite the fact that the 4.0 V amplitude is slightly greater than the coercive voltage distribution in the negative polarity, it remains insufficient to overcome the coercive voltage distribution in the positive polarity observed in pristine state. Consequently, complete wake-up is not achieved under these conditions.

Even though the $2P_R$ does rise to approximately 32 $\mu C/cm^2$ for the 4.0 V, 100 Hz square waveform, the number of cycles is limited at 5000 due to oxide breakdown. The 100 Hz square waveform imposes considerable field stress on the oxide, making it less favorable for achieving substantial post-wake-up remnant polarization while sustaining higher endurance. Using a cycling voltage of 4.5 V results in improved wake-up behavior for all waveforms except the 100 Hz square waveform (Figure 4.3(d) - limited to 2000 cycles), where the higher field strength leads to even lower endurance. Upon further elevating the voltage to 5.0 V, a noteworthy enhancement in wake-up performance is

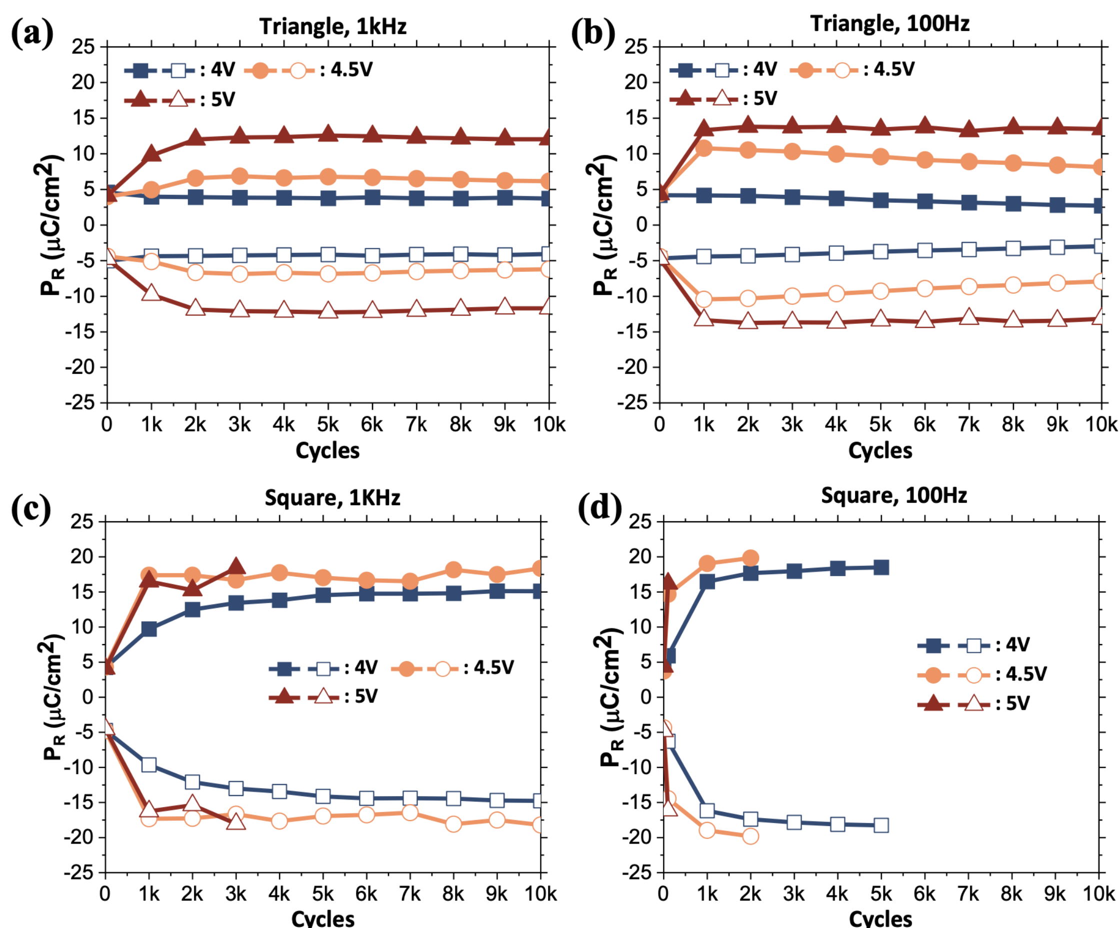

Figure 4.3: (a-d) The evolution of remnant polarization from its pristine state to 10^4 cycles is depicted for the four wake-up waveforms, each employing cycling voltage amplitudes of 4 V, 4.5 V, and 5 V. The PUND P-V measurements are performed using a triangular waveform with frequency 1 kHz and voltage amplitude of ±4.5 V. Figures are reproduced from Nair et al [219].

observed, particularly in the 1 kHz triangular waveform ($2\mathrm{P_R}$ reaching approximately 25 $\mu\mathrm{C/cm^2}$ at 3000 cycles) and the 100 Hz triangular waveform ($2\mathrm{P_R}$ roughly 28 $\mu\mathrm{C/cm^2}$ at 3000 cycles). The enhancement in square waveforms is modest, but it notably affects endurance. For instance, only 3000 cycles can be achieved with the 1 kHz square waveform, and a mere 100 cycles with the 100 Hz square waveform when using 5.0 V. This implies that 5.0 V induces substantial field stress in square waveforms. As previously mentioned, there exists an asymmetry in the coercive voltage distribution between the two polarities, with a lower mean coercive voltage for the negative polarity (approximately -3.0 V, as indicated by the current peak in the switching I-V curves in Figure 4.1). Hence, the application of -5.0 V during each half-cycle of wake-up cycling results in significant field

stress on the oxides, leading to defect formation and ultimately causing fatigue and device breakdown. Therefore, achieving balance between the field stress and wake-up cycles for both polarities is essential, and this will be addressed in the subsequent sections.

As depicted in Figure 4.3, employing a voltage of 4.5 V during cycling demonstrates a reasonable wake-up response across various waveforms. Next, a comparison in wake-up performance among three waveforms, namely, 1 kHz triangular, 100 Hz triangular, and 1 kHz square is made. The 100 Hz square waveform is excluded from consideration due to its limited endurance. Figure 4.4(a) presents the comparison of the evolution of $\mathrm{P_R}$ from pristine state up to 10^4 cycles for these three wake-up sequences. Notably, when cycling with the 1 kHz square waveform, $\mathrm{2P_R}$ reaches the highest value of approximately 35 $\mu\mathrm{C/cm^2}$ after just 1000 cycles, demonstrating remarkable polarization stability that persists up to 10^4 cycles. When utilizing 100 Hz and 1 kHz triangular cycles, the $\mathrm{2P_R}$ values reach approximately 20 $\mu\mathrm{C/cm^2}$ (attained after 1000 cycles) and 14 $\mu\mathrm{C/cm^2}$ (achieved after 2000/3000 cycles) respectively. Additionally, it is worth noting that in both cases, the $\mathrm{P_R}$ begins to decline following the wake-up process. It seems that the onset of fatigue effects occurs at a lower cycle count, and is especially pronounced with the 100 Hz triangular waveform. We observe a comparable fatigue effect when subjecting the system to sub coercive voltage cycling at 3.0 V for all three considered waveforms (as shown in Figure 4.2). This fatigue phenomenon, which arises from inadequate wake-up, resembles the findings reported by Li et al. [223]. In their study, insufficient wake-up, resulting from partial switching due to lower voltage or shorter pulse width in the square waveform, led to an increased fatigue response in the Pt/HZO/LSMO/STO stack. This was attributed to an elevated concentration of domain walls and the pinning of domains caused by charged defects. A similar mechanism may be at work in the case of triangular waveform cycling studied here.

In their study, Starschich et al [216] emphasized that the key factor influencing wake-up in TiN-(Y doped) HfO_2-TiN (M-FE-M) capacitor stacks is the duration of the applied electric field, rather than of the total cycle count. That work exclusively examined the impact of square waveforms with different frequencies, with symmetric negative and positive voltage amplitudes. In order to understand the impact of duration of the applied electric field and cumulative number of cycles, we have plotted $\mathrm{P_R}$ dependency on both

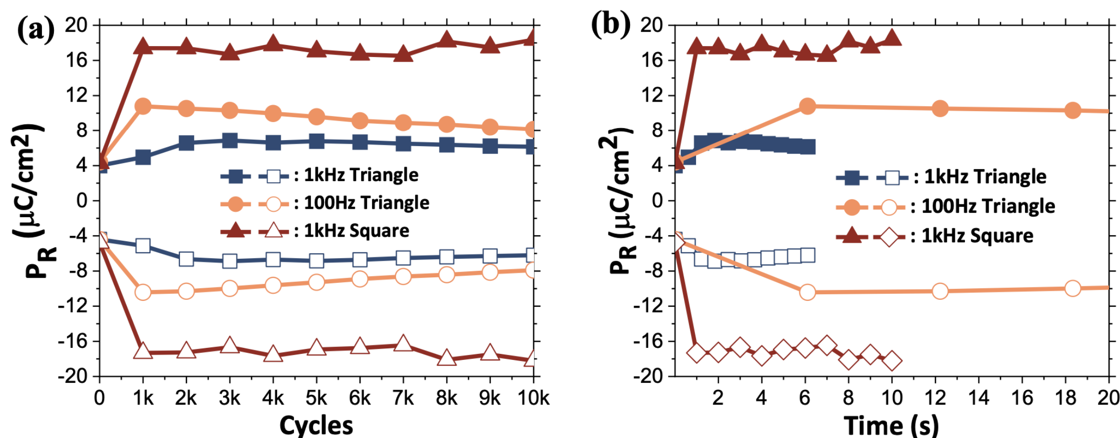

Figure 4.4: (a) The evolution of remnant polarization from its pristine state up to 10^4 cycles is depicted for the three different wake-up waveforms. (b) The evolution of polarization over time is shown. For square waveform cycling, time is computed as the product of the number of cycles and pulse width. In the case of triangular cycling, the time duration corresponds to the period in which the device is exposed to a voltage amplitude exceeding 1.75 V. This threshold voltage signifies the point at which the switching current in the I-V curve begins to rise (as illustrated in Figure 4.1(c) and (d)), indicating the initiation of domain switching. Figures are reproduced from Nair et al [219].

of these parameters in Figure 4.4 The relationship between P_R and number of cycles is shown in Figure 4.4(a). For the same number of cycles, square waveform has higher P_R than both the triangular waveforms. Now, the dependence of P_R with the duration of the applied electric field for the three waveforms is shown in Figure 4.4(b). In the case of triangular waveforms, we focus on the period during which the voltage amplitude exceeded 1.75 V, which coincides with the point where the switching current in the I-V curves begins to rise (as observed in Figure 4.1(c)-(e)). It is evident that P_R is higher for square waveform compared to both the triangular ones for the entire duration of waveform application. In terms of voltage amplitude in every cycle, it should be noted that in the square waveform, the voltage amplitude remains constant at $\pm$4.5 V while in triangular waveforms, the voltage undergoes continuous changes, with the voltage exceeding 4.0 V for only a brief period within each cycle. This aspect will be an important point to understand the difference in switching dynamics between the two waveform types. From the measurements, it is clear that the P_R depends strongly on the waveform type rather than the duration of applied electric field. This is one of the significant findings of this experimental work.

In order to understand the underlying mechanism that brings about the observed dif-

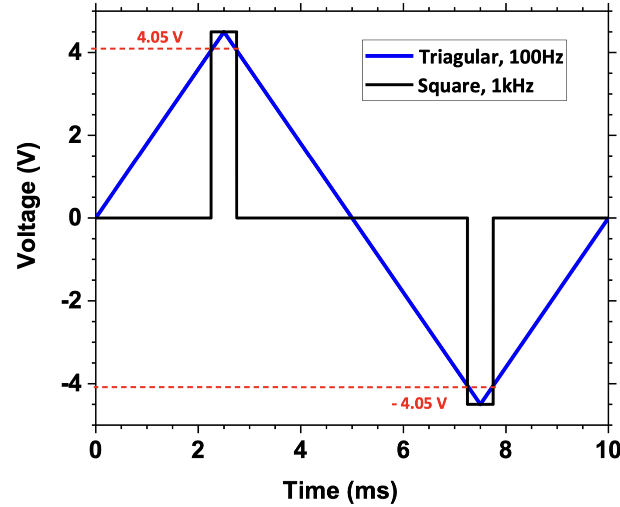

Figure 4.5: Comparison of the amplitude of voltage with time for positive and negative polarity half cycles for square 1 kHz and triangular 100 Hz waveforms. The half cycles of the square waveform are depicted specifically around the amplitude peaks of the 100 Hz triangular wave for clarity. In the 1 kHz square waveform, the amplitude reaches +4.5 V for positive polarity and -4.5 V for negative polarity half cycles, each lasting 0.5 ms. Meanwhile, during this duration, the amplitude in the 100 Hz triangular waveform exceeds 4.05 V for the positive polarity half cycle and falls below -4.05 V for the negative polarity half cycle. As a result, both the 1 kHz square and 100 Hz triangular waveforms maintain a voltage amplitude exceeding 4 V for 0.5 ms in each half cycle.

ference in wake-up in the two waveform types, we try to develop a hypothesis based on the switching dynamics that happen in each switching cycle. First considering pristine state, the coercive voltage distribution extends to around -4.0 V for the negative polarity, based on the minimum of the switching current peak observed in Figure 4.1(c)-(f). Therefore, we assume that during both the triangular and square waveforms, all domains switch from a downward to an upward orientation, since the maximum applied amplitude is -4.5 V. Now, considering the positive polarity coercive voltage distribution, we observe that it extends beyond 4.0 V. The switching current continues to reduce above 4.0 V (in Figure 4.1(c)-(f)), indicating that the switching process is yet not complete. The difference in wake-up observed could stem from the difference in switching events above 4.0 V, as this region is where the effective electric field among the waveforms might be different. For the 1 kHz square waveform within the positive polarity half-cycle, the voltage exceeds 4.0 V for a duration of 0.5 ms. In the case of the 100 Hz triangular waveform, it surpasses the 4.0 V threshold for nearly 0.55 ms (as shown in Figure 4.5). Although, both the 100 Hz triangular and 1 kHz square waveforms have voltages exceeding 4.0 V for a

similar duration, the resulting $\mathrm{P_R}$ after wake-up significantly differs between these two scenarios. The presence of a consistently higher effective voltage in the square waveform (4.5 V for the entire 0.5 ms during the positive polarity half-cycle) appears to play a crucial role in the wake-up mechanism. Moreover, the wider coercive voltage distribution observed for positive polarity in the pristine state (as depicted in Figure 4.1(c)-(f)) suggests that some domains may be pinned in a direction pointing toward $\mathrm{Al_2O_3}$. This pinning effect is likely attributed to the presence of traps or vacancies in proximity to the $\mathrm{Al_2O_3}$-HZO interface. Hence, it becomes crucial to release these pinned domains from their positions during the positive polarity half-cycle to facilitate the wake-up process. To quantify this, the root mean square (RMS) value of the voltage amplitude for the 100 Hz triangular waveform within the voltage range of 4.0 to 4.5 V, is calculated. It is equal to 0.2885 V ($= 0.577 \times 0.5$ V). In contrast, the RMS value for the 1 kHz square waveform is 0.5 V. It is worth noting that during the switching process, there is a phenomenon of charge injection from the electrodes to charge traps, leading to the charging or discharging of these traps [224], along with the movement of oxygen vacancies under the applied electric field [210, 225]. Due to the fact that the triangular waveform has a lower RMS voltage, and therefore a reduced effective electric field compared to the square waveform, both the movement of vacancies and charge injection are significantly diminished when subject to the triangular waveform, despite both waveforms experiencing voltage larger than 4.0 V for an equivalent duration.

These mechanisms are illustrated in the schematic presented in Figure 4.6. In its pristine state, when subjected to a switching voltage to shift the polarization from the P-up to the P-down state, not all domains successfully undergo this transition. Some domains remain fixed in the P-up state due to the presence of negatively charged traps. To engage these pinned domains in the P-down switching process, it is crucial to neutralize these charges through either charge trapping/de-trapping or by facilitating their drift/rearrangement in a manner that enables the pinned domains to switch. Both of these processes become more pronounced (involving higher rate of charge trapping/de-trapping or charge trap movement over greater distances) at higher electric fields. As a result, the higher voltage experienced during the positive polarity phase in the 1 kHz square waveform, in comparison to the 100 Hz triangular waveform, amplifies the wake-up process in

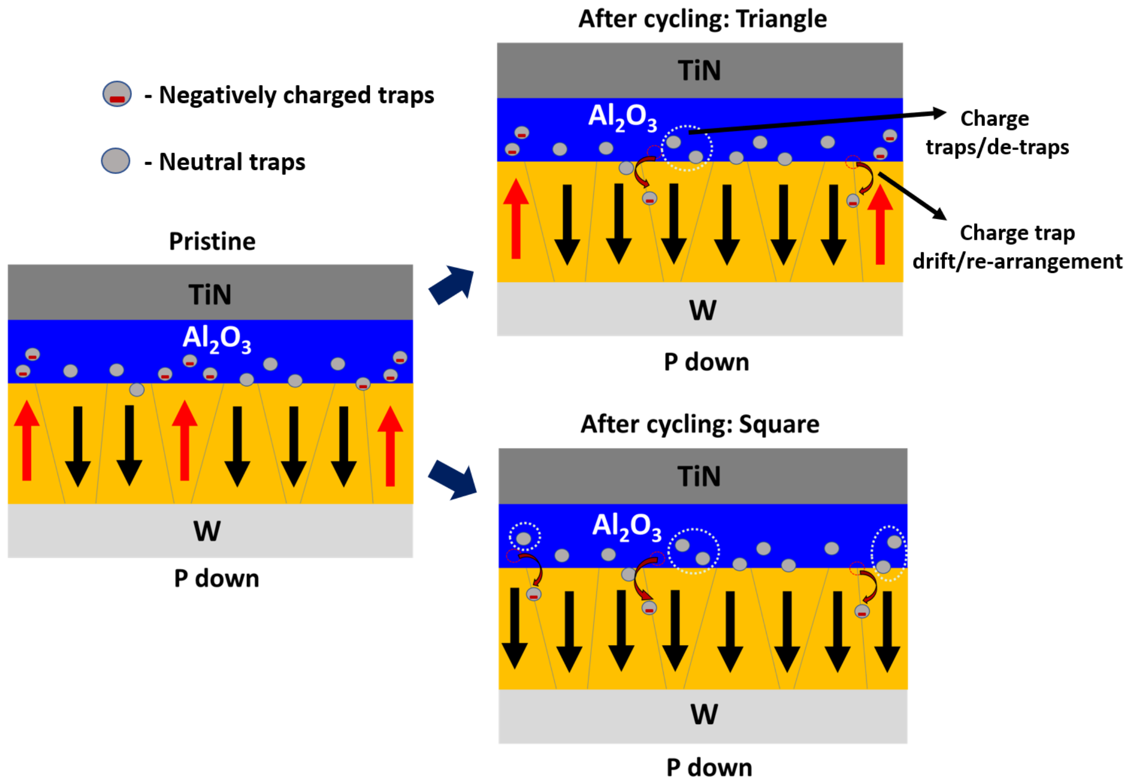

Figure 4.6: This schematic illustrates the mechanism responsible for the increased remnant polarization following square waveform cycling.

square waveforms. This observation indicates the significant influence of charges situated in the vicinity of the Al_2O_3-HZO interface on the wake-up characteristics of bilayer FTJ stacks.

The wake-up P_R is highly dependent on the type of waveform used for the cycling operation. Here, we discuss how the different cycling waveforms influence the coercive voltage of the polarization switching mechanism. Figure 4.7 (a)-(d) shows the evolution of coercive voltage from pristine to 10^4 cycles for the four waveforms used for performing the wake-up operation as shown in Figure 4.1(b). The coercive voltage values are extracted from the PUND P-V measurements. For all the cycling waveforms, the coercive voltage shifts to lower magnitude in the positive polarity and to higher magnitude in the negative polarity when cycled from pristine to 10^4 cycles. In case of triangular 1 kHz (Figure 4.7 (a)), with the increase in the switching voltage amplitude, the coercive voltage decrease is more pronounced. In case of triangular 100 Hz (Figure 4.7 (b)), the decrease in coercive voltage from pristine to 10^4 cycles increases when the voltage amplitude is increased to 4.5 V from 4.0 V. When the voltage amplitude is further increased to 5.0 V,

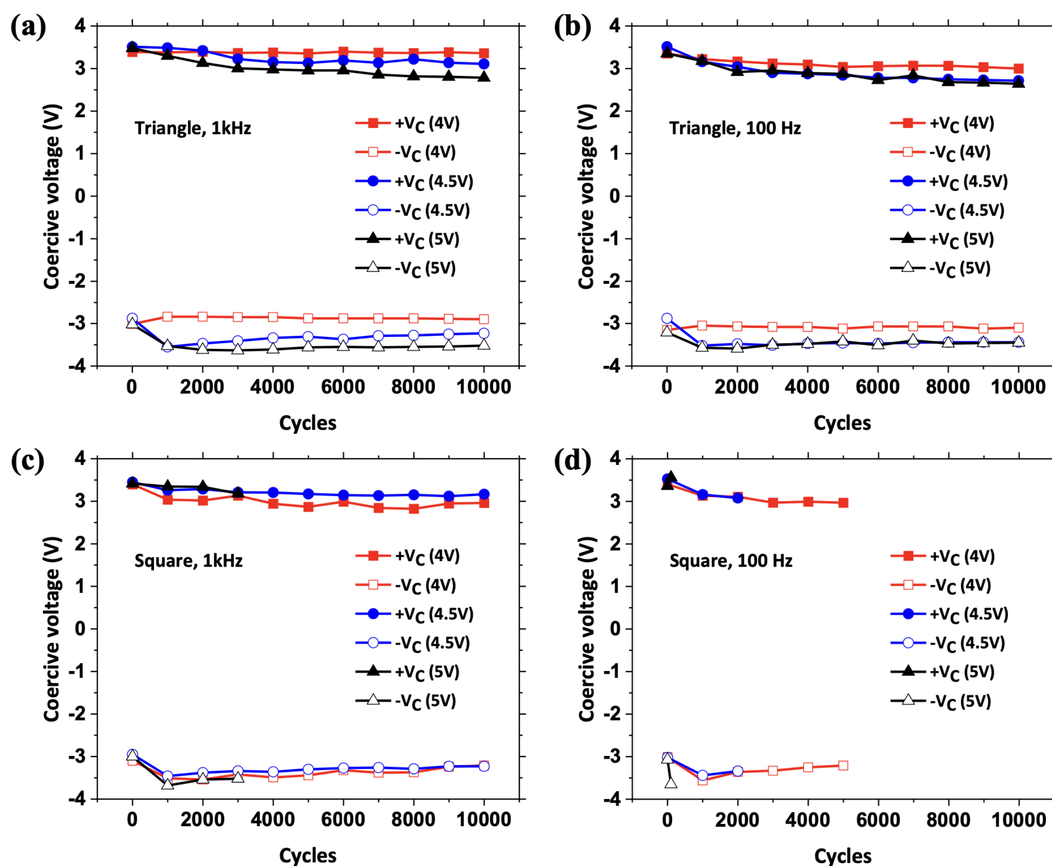

Figure 4.7: (a-d) The evolution of coercive voltage (V_C) from its pristine state to 10^4 cycles is depicted for the four wake-up waveforms shown in Figure 4.1 (b), each employing cycling voltage amplitudes of 4.0 V, 4.5 V, and 5.0 V.

there is no further decrease of coercive voltage. The curves corresponding to 4.5 V and 5.0 V overlaps fairly well. In case of square 1 kHz (Figure 4.7 (c)), there is no clear trend of change in coercive voltage as a function of the switching voltage amplitude. For square 100 Hz (Figure 4.7 (d)), the curves corresponding to 4.0 V and 4.5 V switching amplitudes overlap. In this case, 4.0 V is sufficient to create the decrease in coercive voltage completely and increase in voltage leads to smaller endurance.

In order to understand the influence of wake-up cycling waveforms on the memory functionality of the FTJ devices, the tunneling current was measured from pristine to 10^4 cycles following both Reset and Set operations for each waveform sequence. Reset and Set operations were executed using triangular pulses with a width of 0.5 ms and amplitude of +4.5 V and -4.5 V, respectively. These operations were conducted subsequently to the application of the cycling waveform for a specified number of cycles. The OFF state current (measured post-Reset operation) and ON state current (measured after the Set op-

eration) were obtained by applying a constant read voltage of -1.6 V for a duration of 500 ms. The current value is an average taken over this period. The sequence of measurements is depicted in Figure 4.8(a). The energy band diagram schematics corresponding to the Set and Reset states under the applied read voltage are illustrated in Figure 4.8(b) and (c), respectively.

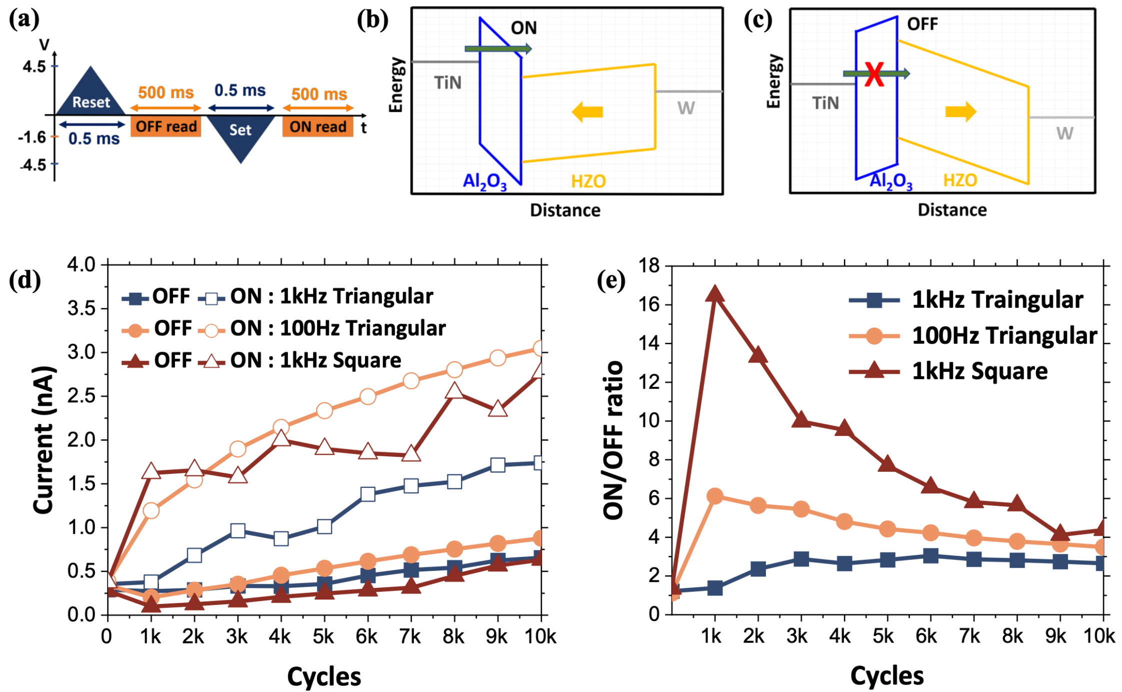

Figure 4.8: (a) The pulse sequence employed to measure OFF and ON state currents involves Reset and Set operations conducted with 0.5 ms width triangular pulses at +4.5 V and -4.5 V, respectively. The read measurement is carried out with a DC voltage of -1.6 V. (b) Energy band diagram schematic corresponding to the ON state (polarization directed towards Al_2O_3; -P_R). (c) Energy band diagram schematic corresponding to the OFF state (polarization directed towards the bottom W metal; +P_R) under the read voltage bias.(d) The evolution of ON and OFF state currents over cycles for the three cycling waveforms. (e) The evolution of the ON/OFF ratio over cycles for the three different wake-up cycling waveforms. Figures are reproduced from Nair et al [219].

As discussed in chapter 1 Section 1.2, the ON and OFF currents are influenced by the depolarization field within the HZO layer, which is directly proportional to the remnant polarization value [127] (assuming the charge traps at the interface do not completely neutralize the bound charges [226]). The smaller remnant polarization resulting from 1 kHz triangular waveform cycling leads to a lower ON current and to the lowest ON/OFF ratio, as shown in Figure 4.8(d) and (e). In contrast, both 100 Hz triangular and 1 kHz square waveform cycling yield higher ON currents. The high remnant polarization achieved with

1 kHz square waveform cycling, results in the highest ON currents and lowest OFF currents, culminating in the highest ON/OFF ratio of 17 among the three cycling waveforms.

All the three waveforms exhibit an increase in both ON and OFF currents with cycles, signaling the emergence of defects and the onset of fatigue (Figure 4.8(d)), it is observed that the OFF current associated with 1 kHz square cycling consistently remains the lowest among the three waveforms. However, it is worth mentioning that there is a notable reduction in the ON/OFF ratio within the square waveform after 1000 cycles (from 17 at 1000 cycles to approximately 5 at 10^4 cycles). Given that this waveform results in a high $\mathrm{P_R}$, it can be inferred that the stack sustains the highest depolarization field among the three sequences. This depolarization field could range from 0.5 to 1 MV/cm, causing the generation of defects over cycles [210], consequently elevating the OFF state current and reducing the ON/OFF ratio. Even with this decrease, square waveform cycling still yields a superior ON/OFF ratio up to 10^4 cycles, a higher ON-OFF current value (enabling more intermediate states), and enhanced stability over cycles. This demonstrates the intricate interplay between high $\mathrm{P_R}$ and the onset of fatigue in bilayer FTJ devices.

As discussed earlier, we observe that, a higher effective voltage during the positive polarity half-cycle in the 1 kHz square waveform cycling leads to the switching of a greater number of previously pinned domains, resulting in the attainment of the highest $\mathrm{P_R}$ after only 1000 cycles (shown in Figure 4.3). Therefore, one can consider that voltage amplitude greater than 4.5 V or larger pulse width may be necessary to obtain even higher $\mathrm{P_R}$. In order to test this, the devices were subjected to square cycling waveforms of larger pulse width and voltage amplitude. For the case of 100 Hz square waveform approximately 4.5 $\mu\mathrm{C/cm^2}$ higher $\mathrm{P_R}$ (Figure 4.3(c) and (d)) was obtained compared to 1 kHz square waveform for cycling voltage of ± 4.5 V. By increasing the voltage amplitude to ± 5 V (Figure 4.3(d)), a 2$\mathrm{P_R}$ of about 33 $\mu\mathrm{C/cm^2}$ was achieved after just 100 cycles. Whereas for the 1 kHz square waveform, the 2$\mathrm{P_R}$ of $\sim$35 $\mu\mathrm{C/cm^2}$ was obtained only after 1000 cycles. Nonetheless, as depicted in Figure 4.1(c)-(f), we note that the coercive voltage distribution in the negative polarity is narrower, and the average coercive voltage is of lower magnitude. Employing -5 V, for instance, results in an exceedingly high field stress, leading to device failure after 100 cycles for 100 Hz and 3000 cycles for 1 kHz square, ± 5 V cycling operations. Hence, distinct voltage amplitudes are required for the

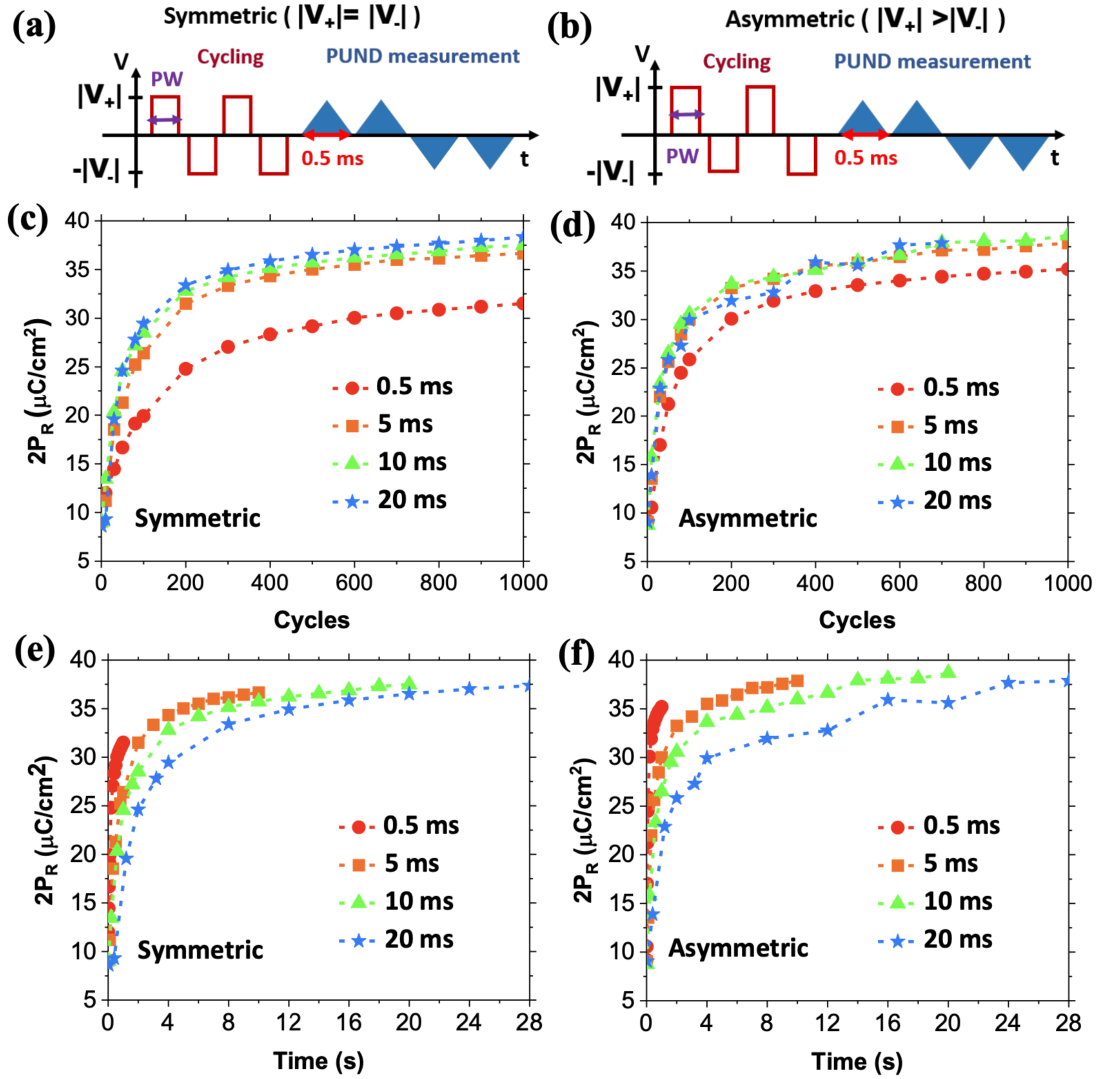

Figure 4.9: Illustration of the measurement sequence corresponding to cycling with (a) a symmetric pulse train, where the amplitudes of the square pulse for both polarities are equal, with $|V_+| = |V_-| = 4.5$ V, and (b) an asymmetric pulse train, where the amplitudes for both polarities are unequal, with $|V_+| = 5.0$ V and $|V_-| = 4.5$ V. Time is calculated as: time = number of cycles $\times$ 2 times pulse width. (c, d) The progression of $2\mathrm{P_R}$ from the pristine state to 1000 cycles for symmetric and asymmetric cycling pulses with varying pulse widths (0.5, 5, 10, and 20 ms). (e, f) The evolution of $2\mathrm{P_R}$ over time for symmetric and asymmetric cycling pulses, respectively. Figures are reproduced from Nair et al [219].

two polarities.

Our instrument lacks the capability to apply a continuous waveform with unequal amplitudes for the two polarities. As a work-around, we generated a cycling waveform by stringing together alternating polarity square pulses, referred to as a 'pulse train'. This measurement sequences, involving equal voltage amplitudes for both polarities, denoted as 'symmetric', and measurements with different amplitudes, referred to as 'asymmetric'. They are depicted in the schematic in Figure 4.9(a) and (b). The polarization behavior of the devices subjected to symmetric (V_+ = 4.5 V, V_- = -4.5 V) and asymmetric (V_+ = 5.0 V, V_- = -4.5 V) pulse train cycles is illustrated in Figure 4.9(c) and (d), respectively, for various pulse widths of 0.5, 5, 10, and 20 ms. Figure 4.9(c) demonstrates an enhancement of $2P_R$ over cycles for the symmetric cycling pulse train with varying pulse widths. As the pulse width increases, the wake-up ($2P_R \sim 32\mu C/cm^2$) occurs in fewer cycles, with a particularly notable improvement between 0.5 and 5 ms. In the case of asymmetric pulse train cycling, the difference in wake-up for different pulse widths is minimal, as indicated in Figure 4.9(d). Comparing the 0.5 ms pulse width cycling for symmetric and asymmetric cases, we observe that wake-up occurs in about 400 cycles for the asymmetric case, whereas the symmetric case necessitates nearly 1000 cycles. This demonstrates a clear advantage of asymmetric cycling in terms of number of cycles required for wake-up. The reduction in wake-up cycles may be attributed to depinning, thereby enabling the switching of a larger number of domains during each positive polarity half-cycle.

In order to understand whether wake-up is influenced by cycles or by the duration of electric field application, Figure 4.9(e) and (f) present the $2P_R$ value over the duration of the applied field (cycles × pulse width) for the symmetric and asymmetric pulse trains, respectively. In the case of the symmetric pulse train, the remnant polarization reaches similar values after approximately 10 seconds for various pulse widths. However, with the asymmetric pulse train, the increase in the $2P_R$ value over time varies significantly for different pulse widths. Notably, even with the shortest pulse width (0.5 ms), a high $2P_R$ of about 35 $\mu C/cm^2$ is attained. Given the disparity in how P_R evolves with time between symmetric and asymmetric pulses, it is evident that a higher positive voltage in the asymmetric configuration accelerates the wake-up process in the HZO layer.

Given that asymmetric pulse train cycling leads to higher remnant polarization in

fewer cycles, it has been selected for further investigation and optimization of ON and OFF currents as well as the ON/OFF ratio. As observed in Figure 4.9(d) for the asymmetric case, wake-up occurs in around 200 cycles with a pulse width of 5 ms, and there is no further increase in remnant polarization with an increase in pulse width.

Three pulse train sequences (designated as A, B, and C) were studied with different voltage amplitudes and two pulse widths (0.5 and 5 ms), as depicted in Figure 4.10(a). Here, Reset and Set operations were executed using square monopolar pulses of +4.5 V and -4.5 V amplitudes, respectively. OFF and ON state current measurements were conducted by applying a constant voltage of -1.6 V. Sequence A contains a cycling pulse train waveform with +5 and -4.5 V amplitudes and a pulse width of 0.5 ms. In this sequence, the same pulse train was used to cycle the device from pristine to 1000 cycles. For sequence B, cycling from pristine to 100 cycles was carried out with a square pulse train waveform featuring +5 and -4.5 V amplitudes and a pulse width of 0.5 ms. From cycle 101 to 1000, the voltage amplitudes were altered to +4.75 and -4.5 V. Sequence C is similar sequence B, except a pulse width of 5 ms (instead of 0.5 ms) was employed for cycling from pristine to 100 cycles. Between sequences A and B, the only modification was the reduction of the positive polarity cycling voltage amplitude to +4.75 V after 100 cycles. As evidenced in Figure 4.10(b) and (c), this reduction had no impact on the ON current but exhibited a beneficial effect in reducing the OFF current. The higher negative polarity voltage amplitude in sequence A potentially led to defect generation, hence triggering the onset of fatigue in the FTJ after only 100 cycles. It is hypothesized that the increase in OFF current serves as a reliable indicator of fatigue and defect generation within the stacks.

Based on the band configuration in the OFF state (Figure 4.8(c)), an elevation in OFF current could stem from either diminished polarization or an augmentation in defect states within the band gap of Al_2O_3 and/or HZO. As P_R continues to increase after 100 cycles in sequence A, the increase in OFF state current may be attributed to defect generation. Hence, sequences B and C exhibit a delay in the onset of the fatigue effect. With a lower OFF current, the ON/OFF ratio is increased and remains elevated for a greater number of cycles. In sequence C, the initial wake-up phase (from pristine to 100 cycles) is enhanced by increasing the pulse width from 0.5 to 5 ms. As illustrated in Figure 4.10(d), such

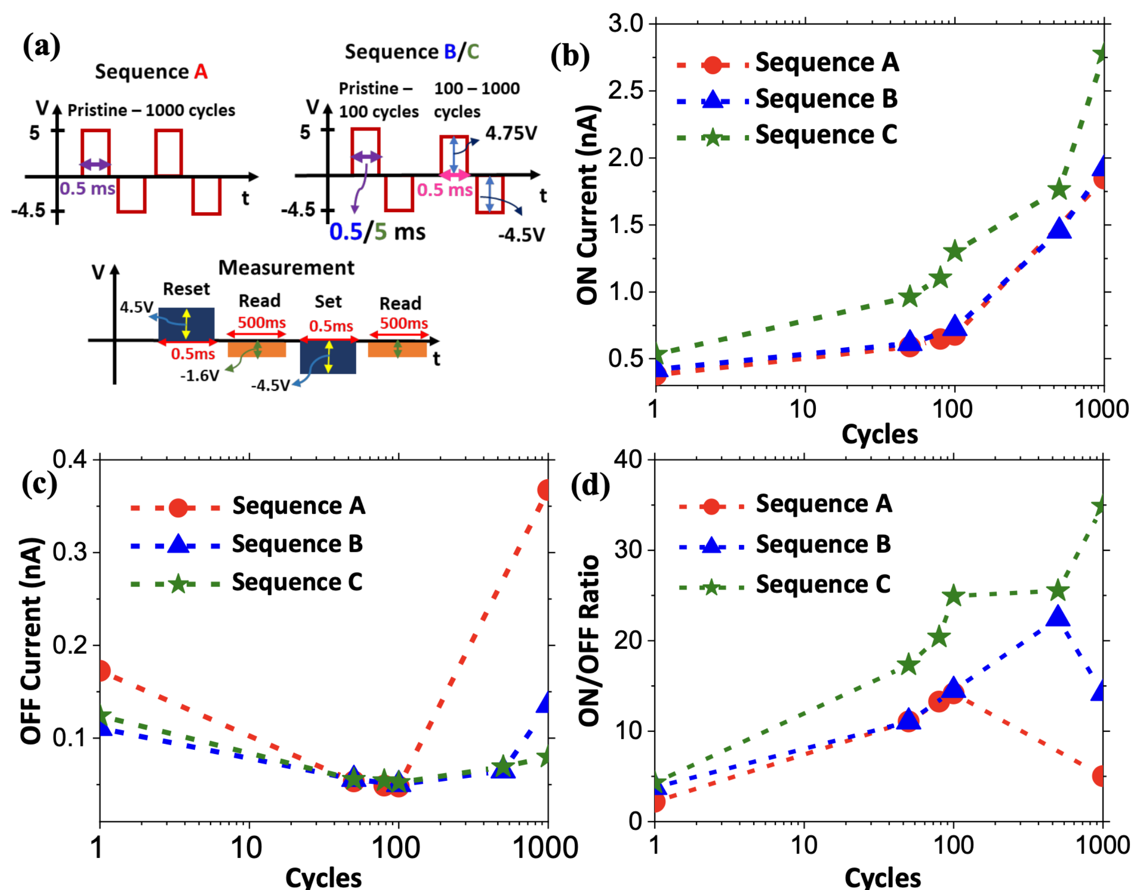

Figure 4.10: (a) The cycling and measurement sequences employed to investigate the influence of cycling pulses on ON and OFF currents. Sequence A involves asymmetric cycling with +5 and -4.5 V using a pulse width of 0.5 ms, conducted from pristine to 1000 cycles. Sequence B encompasses asymmetric cycling with +5 and -4.5 V using a pulse width of 0.5 ms, performed from pristine to 100 cycles, followed by asymmetric cycling with +4.75 and -4.5 V using a pulse width of 0.5 ms from cycles 101 to 1000. Sequence C mirrors sequence B, except for the use of a 5 ms pulse width during the first 100 cycles. Reset and Set operations are executed with +4.5 and -4.5 V square pulses with a pulse width of 0.5 ms. The read operation for the OFF and ON states employs a DC bias of -1.6 V. (b, c) The progression of ON and OFF currents, respectively, from pristine to 1000 cycles for pulse sequences A, B, and C. (d) The evolution of the ON/OFF ratio from pristine to 1000 cycles for pulse sequences A, B, and C. Figures are reproduced from Nair et al [219].

Reference	FTJ structure	ON/OFF ratio
Bilayer		
This work	TiN/HZO/Al_2O_3/W	35
Max. B *et al.* [119]	TiN/HZO/Al_2O_3/TiN	10
Shekhawat. A *et al.* [227]	p-Ge/Al_2O_3/HZO/TiN	14
Ryu. H *et al.* [121]	p-Si/HZO/Al_2O_3/Ti/Au	5
Liu. Y *et al.* [228]	Pt/ZrO_2/HZO/Al_2O_3/ HZO/ZrO_2/Ti/Au	14.8
Bécon-Lours. L *et al.* [229]	TiN/TiO_2/HZO/TiN	2
Bécon-Lours. L *et al.* [230]	TiN/WOx/HZO/TiN	7
Sulzbach. L *et al.* [231]	LSMO/HZO/Al_2O_3/Pt; LSMO/HZO/STO/Pt	700% (7); 390% (3.9)
Cao. V *et al.*, [142]	p+Si/ZrO_2/HZO/Al_2O_3/Ti/Au	31
Lieher. M *et al.*, [232]	TiN/Al_2O_3/HZO/TiN	6
Lin. H *et al.*, [233]	TiN/HZO/MgO/W	32
Wang. H *et al.*, [234]	Si/TiN/HZO/SiO_2/Pt	850
Kim. J *et al.*, [235]	n+Si/HfO_2/HZO/Mo	268
Single layer		
Vargas. F. A *et al.* [115]	TiN/HZO/Pt	15
Prasad. B *et al.* [236]	LSMO/HZO/Pt	135 (1nm HZO), 10^5 (2.5nm HZO)
Sulzbach. M. C *et al.* [237]	LSMO/HZO/Pt	340% (3.4)
Sulzbach. M. C *et al.* [237]	LSMO/HZO/Pt	210% (2.1)
Vargas. F. A *et al.* [238]	Pt/HZO/Pt	20
Goh. Y *et al.* [128]	W/HZO/TiN	16
Goh. Y *et al.* [239]	p-Ge/HZO/TiN	20
Mikheev. V *et al.*, [240]	p+Si/HZO/TiN	80
Gao. Z *et al.*, [241]	NSTO/HZO/Pt	2×10^7

Table 4.1: Comparison of ON/OFF ratios for various HZO based bilayer and single layer FTJ stacks

an increase leads to a substantial improvement in the ON/OFF ratio, resulting in a high value of 35 at 1000 cycles. Although single-layer HZO FTJs demonstrate much higher ON/OFF ratios, it is worth noting that similar bilayer stacks typically achieve ON/OFF ratios ranging from 5 to 32, as summarized in Table 1. Recent studies by Wang H. et al. [234] and Kim J. et al. [235] have demonstrated higher ON/OFF ratios of 850 and 268, respectively, in bilayer FTJ stacks with a ferroelectric HZO layer. However, it should be noted that these high ON/OFF ratios were achieved using RTP annealing temperatures of 750°C and 600°C, respectively. Our approach in engineering the waveform, with an asymmetric amplitude for the wake-up cycling results in a record ON/OFF ratio value with a relatively low crystallization temperature of 400 °C, which makes it fully CMOS

BEOL compatible.

4.3 Reset, Set pulse modification for multiple resistance states stabilization

For synaptic application, the tunneling resistance needs to be tunable to emulate biological synaptic weights. Biological synapses can strengthen or weaken their connections based on the strength and frequency of electrical signals they receive, a phenomenon known as synaptic plasticity [242]. This plasticity enables the human brain to adapt, learn, and store information efficiently. Mimicking the remarkable capabilities of biological synapses, such as synaptic plasticity and learning, is a pivotal goal in the field of artificial intelligence and neuromorphic computing. To replicate these processes in artificial neural networks, the ability to adjust the tunneling resistance of FTJs to various stable values are crucial [243].

The HZO ferroelectric layer contains multiple domains, allowing for a gradual switch of polarization from one direction to the other through controlled switching of individual domains, a few at a time. This is shown in Figure 4.11. Each of these intermediate polarization states leads to distinct intermediate resistance states, giving rise to multiple resistance states. The gradual switching or partial switching of domains can be achieved by performing Reset and Set operations with varying pulse amplitude, pulse width as well as by applying the same pulse multiple times [121]. In this section, we demonstrate multiple resistance states on our CMOS BEOL compatible FTJ device with TiN-Al_2O_3-$Hf_{0.5}Zr_{0.5}O_2$-W architecture (schematic shown in Figure 4.1(a)). Here, we perform polarization switching with sub-switching pulses to attain intermediate polarization states, resulting in intermediate resistance states of the FTJ devices.

Before performing partial switching measurements, the device is woken up with optimized pulse sequence (referred to as sequence C in Figure 4.10(a)) to attain high ON/OFF ratio. The partial switching of the domains were then performed on the FTJ device, resulting in various resistance states, as depicted in Figure 4.12. Two distinct sequences were used for partial switching: (a) a gradual increase in Set or Reset voltage amplitudes while keeping the pulse width constant (Figure 4.12(a)), and (b) a progressive increment in pulse

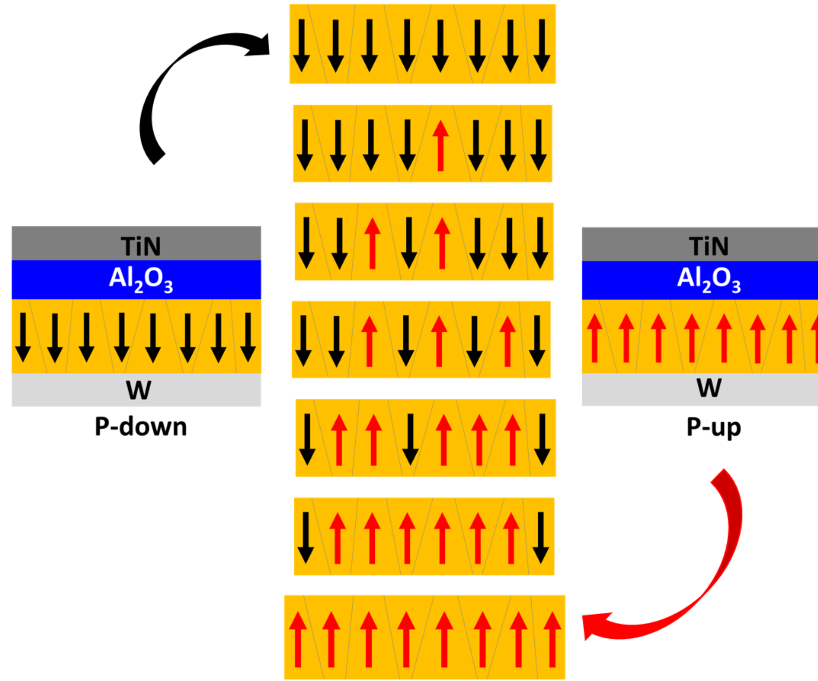

Figure 4.11: Schematic representation of the switching of ferroelectric domains in the HZO layer gradually from one polarization direction to the other.

width for the Set or Reset pulses with a constant voltage amplitude (Figure 4.12(b)). The read current was measured after each partial switching operation involving Reset and Set pulses. The enhancement of conductivity in the FTJ device through the use of modified Set pulses is termed potentiation, while the reduction in conductivity through the application of modified Reset pulses is referred to as depression. This partial switching methods resulted in several clearly defined current states (resistance states) caused by different polarization states, each distinctly separated by over 200 pA.

In Figure 4.12(c), it is evident that at least six distinct current states were observed for both Reset and Set operations. These states are achieved with pulse amplitudes ranging from 2.5 to 4 V for the Reset operation (red line), and from -3.25 to -3.75 V for the Set operation (blue line). Likewise, up to eight states are achieved in Set operation in Figure 4.12(d), for pulse widths ranging from 1 to 100 ms. A slight reduction in ON current for pulse widths exceeding 300 ms is noticed in Figure 4.12(d). As discussed in reference [206], this could be attributed to an overcompensation of bound polarization charges due to the charging/discharging of traps. This leads to a decrease in band bending and a reduction in tunneling current (ON current). For pulse widths surpassing 300 ms, the time scale appears to be adequate for charging/discharging a substantial number of traps,

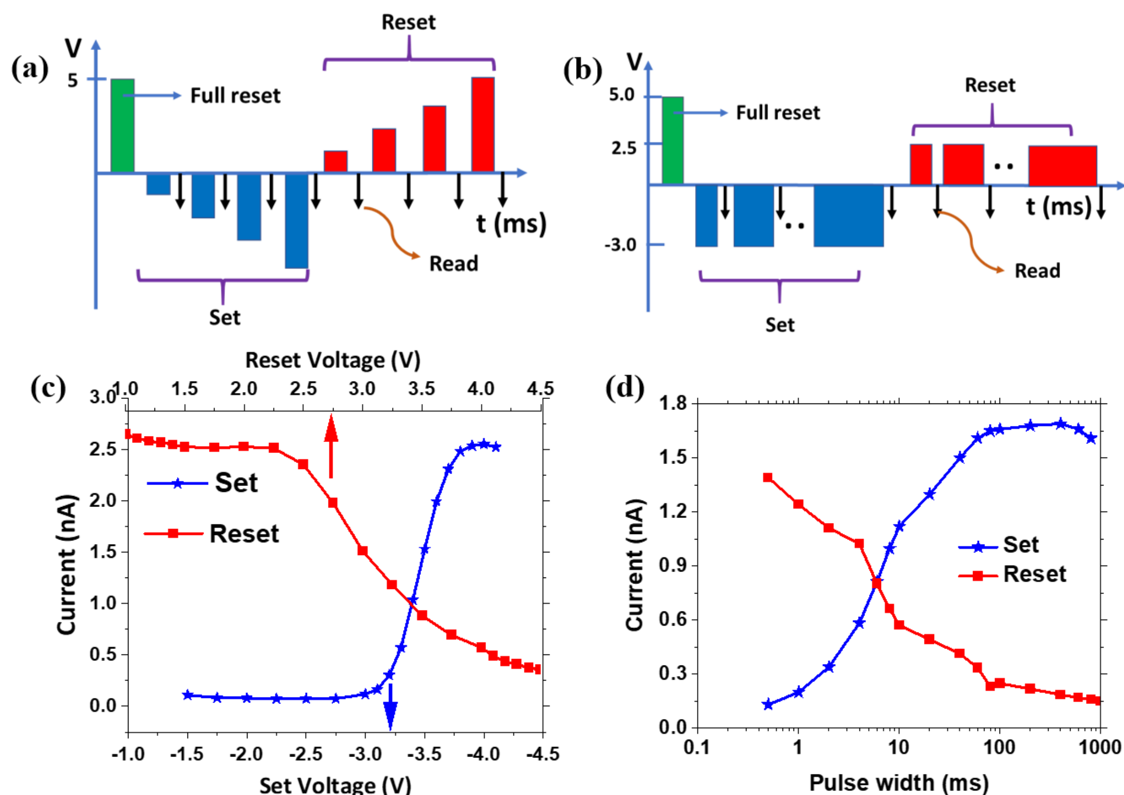

Figure 4.12: Schematic of the pulse scheme used for attaining multiple resistance states in potentiation and depression through (a) pulse amplitude and (b) pulse width modifications. The potentiation and depression attained with pulse scheme in (a) is shown in (c) and the same corresponding to (b) is shown in (d). The partial switching measurements are performed after wake-up (1000 cycles) of the device, where the wake-up cycling operation is performed with optimized sequence C demonstrated in Figure 4.10. Full Reset operation is performed with pulse width of 10 ms. In the depicted sequence (a), both the Set and Reset pulses possess a pulse width of 0.5 ms. Read current measured by applying a DC voltage of -1.6 V. Figures are reproduced from Nair et al [219].

contributing to the overcompensation of bound polarization charges. The multiple resistance states achieved through pulse width and amplitude modifications closely align with the findings of partial switching measurements demonstrated in Ryu et al [121], despite the fact that the pulse width utilized in our experiment is of the order of milliseconds. The Radiant ferroelectric tester tool is used for partial switching measurements. However, applying pulses shorter than 0.5 ms to the devices is not possible due to constraints imposed by the RC time constant.

Ideally, a pulse scheme with constant pulse width and amplitude is desirable to obtain potentiation or depression. With such a pulse scheme, the switching operation is called accumulative switching. Accumulative switching is preferable because it simplifies cir-

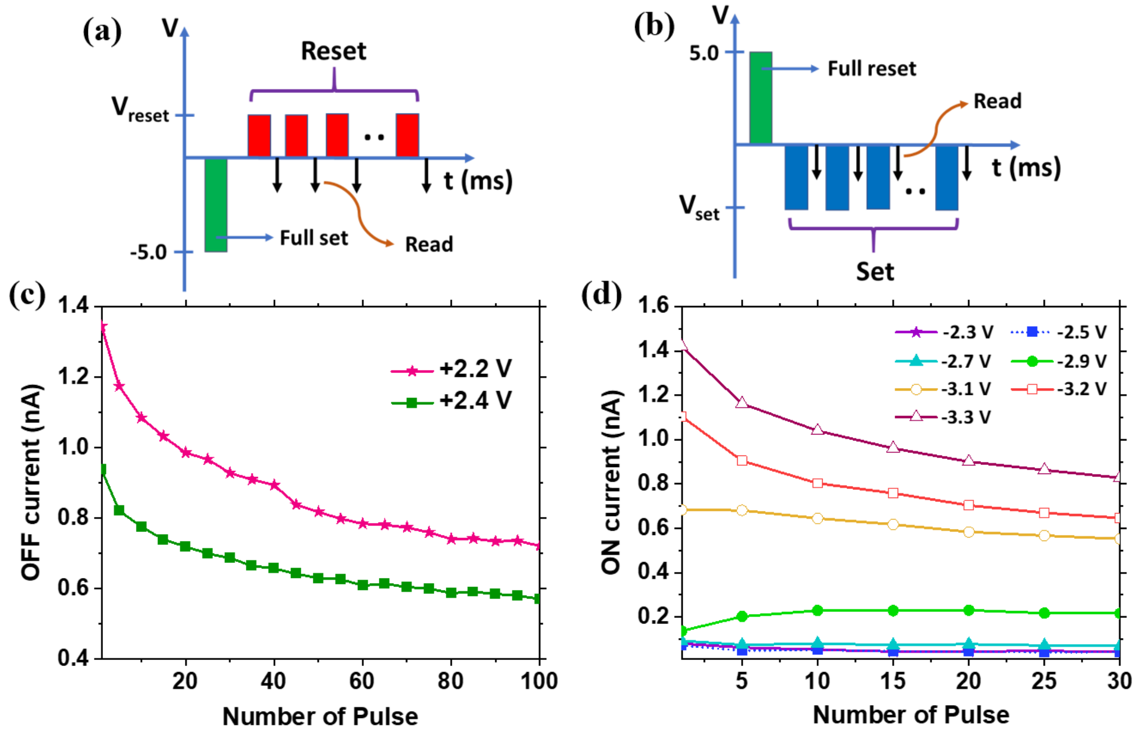

Figure 4.13: Schematic of the pulse scheme used for attaining multiple resistance states in (a) depression and (b) potentiation by applying the same pulse multiple times, known as accumulative switching. Full Reset or full Set operation is performed with pulse of 10 ms pulse width. Reset operation is performed with pulse width of 0.5 ms and Set operation is performed with pulse width of 1 ms. Read measurement is performed by applying DC voltage of -1.6 V after each Reset or Set pulse applied. Depression is achieved with two Reset voltages +2.2 V and +2.4 V and is shown in (c). Potentiation measurement is performed with Set voltages ranging from -2.3 V to -3.3V as shown in (d).

cuit design by allowing the use of identical pulse trains, which are easier and more area-efficient to generate in CMOS technology. This method eliminates the need for complex circuitry and pre-assessment of the device state, reducing latency and improving overall efficiency [135]. The pulse scheme used for switching the resistance from ON state to OFF state (depression) is shown in Figure 4.13(a) and the same used for switching the resistance from OFF state to ON state (potentiation) is shown in Figure 4.13(b). The measurements are performed after waking up the device with the optimized pulse sequence C as shown in Figure 4.10. Switching the polarization from ON state to OFF state with +2.2 V results in the gradual decrease of OFF current from 1.34 nA to 0.72 nA with 100 pulses as shown in Figure 4.13(c). When +2.4 V is used, the OFF current decreases from 0.93 nA to 0.57 nA with 100 pulses. The increase in Reset voltage amplitude lead to the decrease on OFF current achieved from 1 to 100 pulses. This is due to the fact that more

domains are getting switched to the OFF state with each number of pulses. In order to attain potentiation, partial switching measurement is performed using identical pulses with different Set voltages ranging from -2.3 V to -3.3 V as shown in Figure 4.13(d). Even though these voltages are within the positive coercive voltage distribution, applying multiple pulses does not increase the ON current. There is a slight increase in ON current in the first two pulses when -2.9 V is used. But from the third pulse onward the ON current saturates. Here with the increase in Set voltage amplitude, the ON current corresponding to the first pulse increases, which indicates that more and more domains switch to the ON state with the first applied pulse. But the ON current does not increase in subsequent pulses, rather tends to decrease as in the case of -3.2 V and -3.3 V. The decrease in ON current happens when the ON current is higher than 1 nA to start with. Applying constant voltage pulses one at a time does not facilitate the switching of more and more domains to achieve potentiation, although achieving depression is feasible. To achieve potentiation, it is essential to increase either the pulse width or the pulse amplitude of the Set pulses. The inability to achieve potentiation through accumulative switching can be due to the inability to apply Reset or Set pulses with smaller pulse widths and to precisely control the time delay between the partial switching pulses. Accumulative switching is demonstrated on a 2-terminal field effect device developed in our group [244], allowing to achieve potentiation and depression through identical pulse programming scheme. From this, it is evident that the time between two pulses is critical for achieving multiple resistance states through accumulative switching.

4.4 Summary

Our study shows that the waveform used in cycling significantly influences the wake-up process and the resultant remnant polarization in TiN-Al_2O_3-HZO-W FTJ devices. This in turn strongly affect the FTJ properties. These devices involve distinct interfaces, such as dielectric-ferroelectric and ferroelectric-metal, leading to strong domain pinning in one of the polarization directions. We demonstrate that the effectiveness of the cycling waveform in depinning these domains plays a crucial role in the wake-up effect. Square waveforms outperform triangular waveforms, resulting in a higher remnant polarization post-wake-up. Furthermore, we find that different voltage amplitudes are required to

switch between the two polarization directions for achieving the maximum positive and negative remnant polarization in the stack. By employing an asymmetric waveform for field cycling and adjusting the pulse width, we increase the P_R after wake-up and increase the ON/OFF ratio of the FTJ from approximately 5 to 35. These findings demonstrate the importance of fine-tuning the cycling pulse scheme to attain higher ON/OFF ratios and ON-OFF currents, critical factors for achieving distinct resistance states for neuromorphic computing. Modification of the Reset and Set pulses enables us to attain multiple resistance states in the FTJ device. The pulse modulations in the form of amplitude, pulse width and pulse numbers are demonstrated on the FTJ device where the wake-up cycling is performed with the optimized wake-up cycling waveform. Through this optimized approach, we show the ability to achieve multiple well-separated resistance states in FTJs.

Chapter 5

CMOS integration of FTJ device

5.1 Introduction

In the previous chapters we showed that, the FTJ devices are promising candidate for neuromorphic applications due to its properties like low switching voltages making them less power hungry, non-volatile behavior avoiding the need for frequent programming, high speed of switching enabling real-time processing, scalability which allows dense integration and the ability to emulate various synaptic functions through the controlled polarization switching which leads to multiple resistance states. Still, in order to employ these devices in industry application and commercial purposes, it is crucial for these devices to be CMOS compatible. This brings certain limitations in terms of processing temperatures (400-450 °C) and choice of materials. At temperatures above 450 °C, the materials used in the BEOL processes, such as metal interconnects (e.g., copper) and dielectric layers, can degrade or undergo unwanted reactions, compromising the functionality of the integrated circuit.

At the time of commencement of this work, there were already some literature on FTJ devices based on ferroelectric HZO layers [119, 121]. However, the fabrication of those FTJs typically involved a thermal budget of 500-600 °C . Throughout the course of this study, we used HZO crystallization temperature of 400 °C by keeping the CMOS back-end-of-line integration aspect in mind. Successful integration of the FTJ devices on CMOS platform without causing any damage to the CMOS wafer components and demonstration of the FTJ functionalities remain a pivotal milestone towards the goal of

employing these devices for industry applications.

Recently, TiN/HZO (5 nm)/TiN FTJ devices and TiN/Al_2O_3 (2 nm)/HZO (5 nm)/TiN bilayer FTJ devices, each measuring 100 x 100 nm^2, were implemented on a 300 mm Si-wafer platform [232]. The conduction mechanism and performance of these FTJ devices, fabricated using 65 nm CMOS process technology between metal 1 (M1) and via 1 (V1) layers, were discussed . Even though this study provides valuable insights towards the integration of FTJ devices in the CMOS technology, it did not demonstrate the integration of FTJ devices to the CMOS wafer and thus it did not study the FTJ device performance when integrated to the CMOS transistor. For FTJ-based neuromorphic circuits, it is essential to connect FTJ devices with CMOS transistors [138,245]. Bilayer FTJ devices typically exhibit a low ON current density (0.1-1 $\mathrm{pA}/\mu\mathrm{m}^2$), necessitating some degree of current amplification by the transistors within these neuromorphic circuits. A solution to this issue is proposed in [135], where a 2-transistor-1-capacitor (2T1C) circuit is introduced to amplify the current flowing through the FTJ. In this circuit, a common-source amplifier connection of a 1-transistor-1-capacitor (1T1C) constitutes the crucial sub-circuit required for amplification.

The stack optimization of the FTJ devices and the wake-up waveform optimization have been discussed in Chapter 3 and 4, respectively. Building upon the results from these chapters, we now show the integration of our best performing FTJ device (stack D from Chapter 3) on the CMOS back-end-of-line. In this study, we fabricate and characterize W-Al_2O_3-HZO-TiN FTJ devices on top of a 180 nm CMOS chip obtained from XFAB foundry. Fabrication processes involve multiple steps, including deposition, etching, and annealing as already discussed in earlier chapters. Experimental testing is crucial to confirm that the fabrication processes required for FTJ devices are compatible with the existing CMOS BEOL processes, ensuring that there are no adverse effects, such as chemical reactions or structural degradation, that could compromise the device's performance or the integrity of the CMOS circuits. Additionally, we integrate an FTJ with a nMOS transistor on the front-end to demonstrate a 1T1C circuit. Characterization of stand-alone FTJ device (not connected to transistors) is conducted to comprehend its performance when integrated into the CMOS BEOL, in terms of polarization switching, OFF, ON currents and ON/OFF ratio. Recognizing that any BEOL process involving high temperatures

may affect the transistors on the front-end, transistor characterization is performed both before and after the FTJ integration to evaluate the potential impact of the FTJ integration process. Finally, we measure the 1T1C circuit to demonstrate FTJ current amplification.

5.2 Fabrication of FTJ devices on CMOS chip

We received the 180 nm CMOS wafer from the XFAB foundry with 3rd via level (referred to as V3) as the top layer. The wafer was coated with a resist for the protection of wafer surface from scratches and dirt. To facilitate operations within our laboratory-scale fabrication facility, the CMOS wafer was cut into smaller dies with an area of $2 \times 2 \text{ cm}^2$ (shown in Figure 5.2(a)). The dicing of the CMOS wafer was conducted at NaMLab gGmbH, Dresden. The protective resist, covering the surface of the CMOS chip, was removed using ultrasound with Dimethyl sulfoxide (DMSO), followed by ultrasound treatment with Acetone and Isopropanol. The process flow for fabrication of FTJ devices on the CMOS chip is shown in Figure 5.1. To isolate the bottom electrode of the FTJ device from undesired W plugs underneath, a 10 nm $\mathrm{Al_2O_3}$ isolation oxide layer was initially deposited. When the FTJ stack was fabricated on the CMOS chip without the isolation layer, many devices on the chip failed to function properly due to insufficient isolation. The patterning of the FTJ bottom electrode was performed by photolithography, employing a direct laser writer (Heidelberg Instruments DWL 66+), followed by a 30 nm W deposition through room temperature sputtering, with subsequent W lift-off processing. Subsequently, a 3 nm $\mathrm{Al_2O_3}$ layer and a 10 nm HZO layer were deposited using atomic layer deposition (ALD) at 250 °C. The ALD process utilized TMA precursor for $\mathrm{Al_2O_3}$ and TEMA-Hf and TEMA-Zr precursors for HZO, with water serving as the co-reactant for both layers. The TiN top metal electrode, with a thickness of 30 nm, and the W capping metal, with a thickness of 30 nm, were deposited through room temperature sputtering and lifted off on top of the HZO layer. The entire CMOS chip underwent annealing in a rapid thermal processing (RTP) environment at 400 °C for 180 seconds in an N_2 ambient atmosphere.

For establishing contact with the bottom electrode, a contact was opened by etching the $\mathrm{Al_2O_3}$/HZO layers through a BCl_3-based RIE etching process. To connect the bottom electrode of the FTJ device to the gate of an nMOS transistor in the front-end-of-line, and to establish contacts to the transistor's drain and source, the oxides (13 nm $\mathrm{Al_2O_3}$

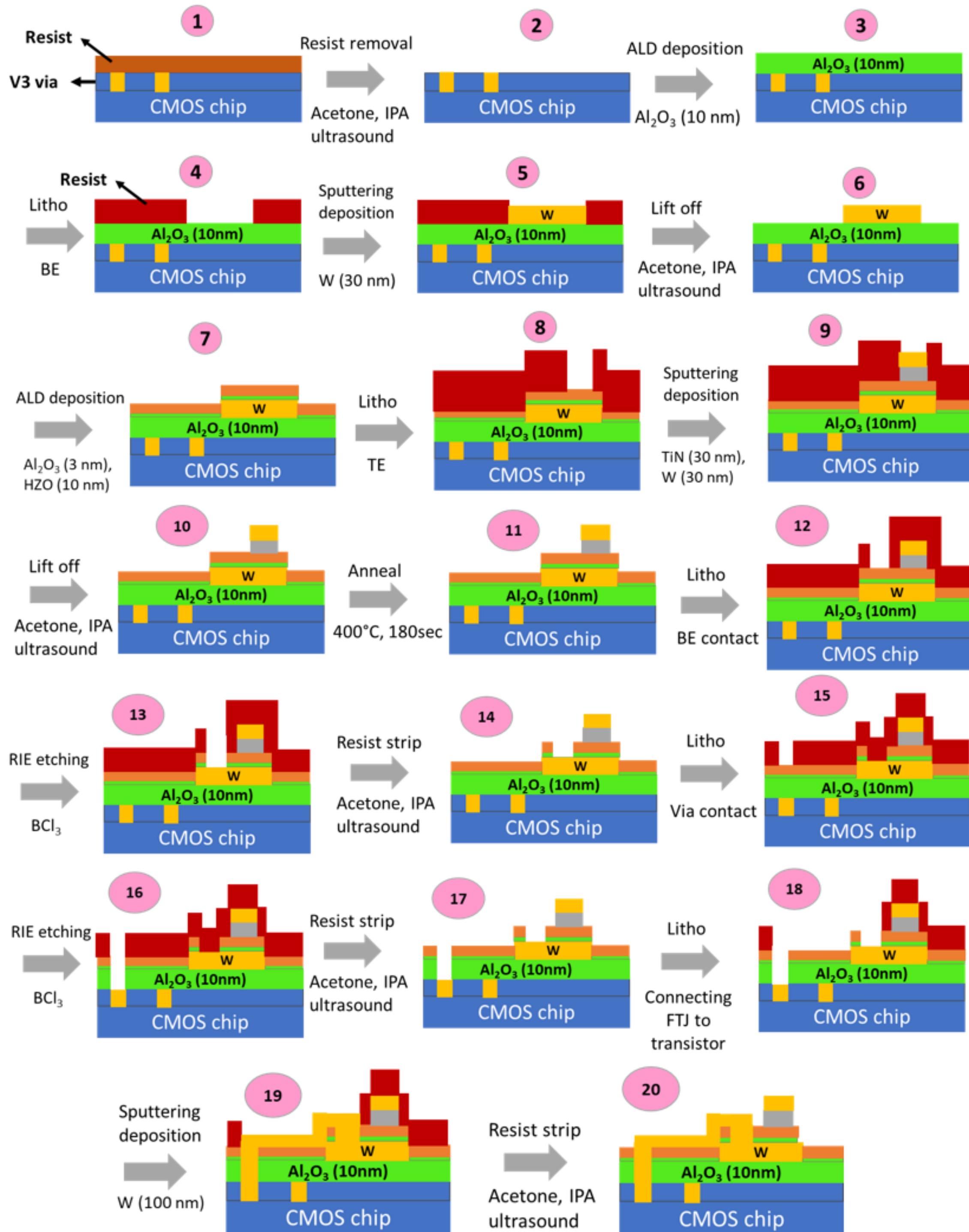

Figure 5.1: (a) The schematic of process flow for FTJ fabrication in the 180 nm CMOS BEOL. The front end (CMOS transistors) including metal layers up to metal 2 are indicated as ‘CMOS chip’. 3rd via level is shown as V3.

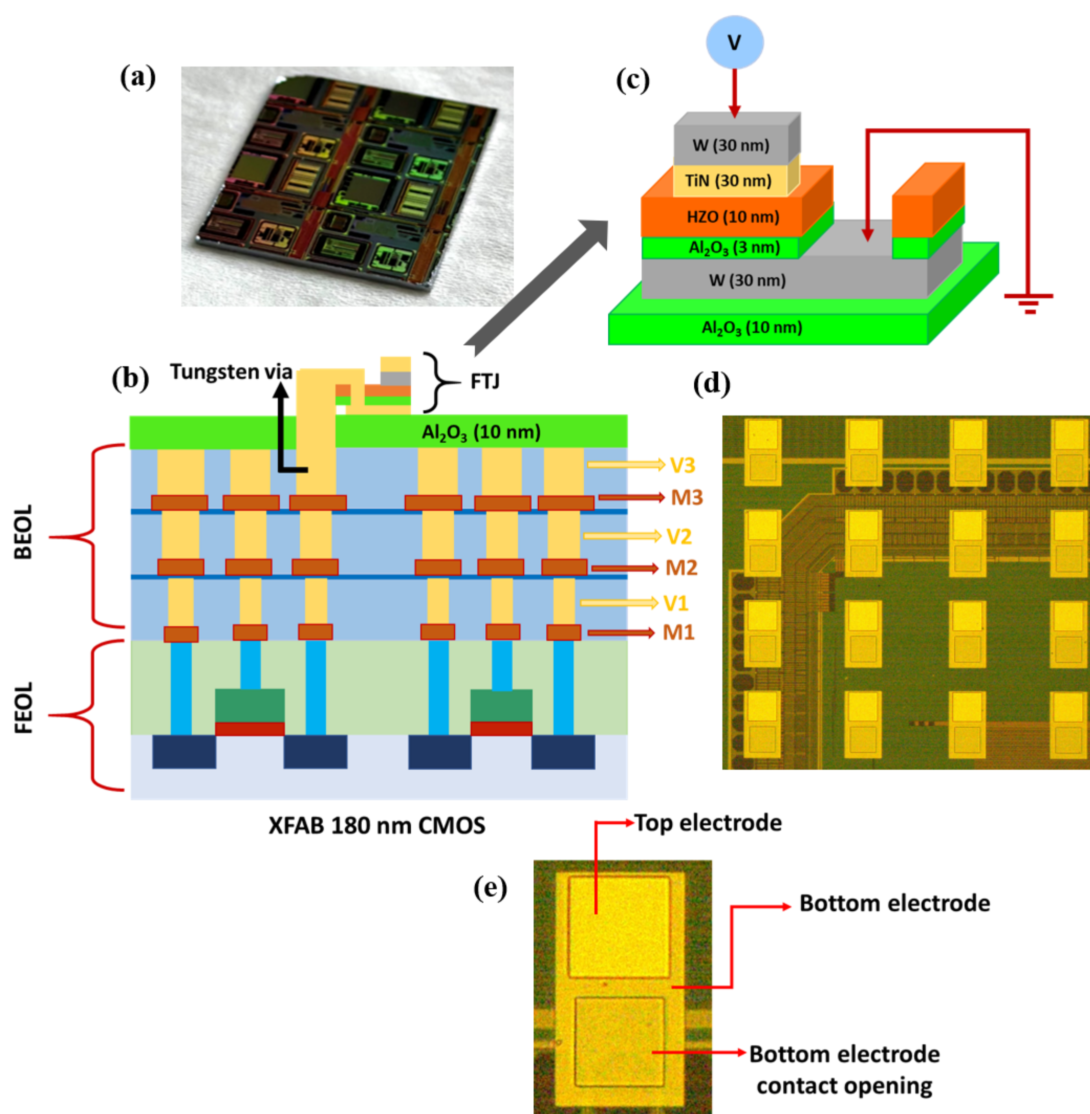

Figure 5.2: (a) A CMOS chip with $2 \times 2\ \mathrm{cm}^2$ dimension. (b) A cross-sectional schematic illustrating the CMOS back-end-of-line (BEOL) stack and the integrated FTJ at the V3 level; (c) A schematic representing the layers of the FTJ device; (d) An optical microscope image from the top view showing stand-alone FTJ devices fabricated on the CMOS chip. (e) Optical microscope image of a single FTJ device. The bottom electrode, top electrode and the bottom electrode contact openings are labelled in the image. The rectangular bottom electrode is of the dimension 110x200 μm^2 . The top electrode is 75x75 μm^2 and the bottom electrode contact is 85x85 μm^2.

and 10 nm HZO) must be etched away from the top of the vias corresponding to the transistor. Contacts were opened above these vias utilizing a BCl_3-based RIE etching process. To establish connectivity between the FTJ and the transistor below, a W line (thickness of 100 nm and width of 25 nm) was fabricated through lift-off, connecting the bottom electrode of the FTJ to the via (in the V3 layer) that extends down to the gate contact of the transistor. In this study, the FTJ is connected to a nMOS transistor in

the front-end, completing a 1T1C circuit. Figure 5.2(b) shows a schematic cross-section of the FTJ device integrated into the CMOS BEOL. The transistors in the front-end-of-line (FEOL) are also shown in the schematic. Figure 5.2(c) provides a schematic of the integrated FTJ device, detailing all its layers. Figure 5.2(d) shows a top-view optical image of multiple standalone FTJ devices. A closer top-view image of a single FTJ device with labeled components is shown in Figure 5.2(e). The bottom electrode is rectangular, measuring $110 \times 200, \mu\mathrm{m}^2$, while the top electrode is $75 \times 75, \mu\mathrm{m}^2$, defining the FTJ device area. To contact the bottom electrode, a square opening of $85 \times 85, \mu\mathrm{m}^2$ is etched through the $\mathrm{Al_2O_3}$ and HZO oxides, located 18.0 $\mu\mathrm{m}$ from the top electrode.

5.3 Stand-alone FTJ characterization

The switching I-V measurements for the W-$\mathrm{Al_2O_3}$-HZO-TiN FTJ device are conducted using the Radiant Multiferroic II tester. These measurements were performed on the stand-alone FTJ device, which is not connected to the transistors. The results are illustrated in Figure 5.3(a) for three different conditions: the pristine state, after 1000 cycles, and after 2000 cycles. The device area was $75 \times 75\,\mu\mathrm{m}^2$. During testing, a triangular voltage with an amplitude of ±5.0 V was applied to the top electrode, while the bottom electrode was grounded. The resulting current through the system was recorded. Additionally, wake-up cycling was performed on the device using a square pulse with ±5.0 V amplitude and a 1 ms pulse width.

In the pristine state, the coercive voltage peak is around 4.0 V for positive polarity (HZO polarization towards $\mathrm{Al_2O_3}$, ON state). However, in negative polarity (with HZO polarization away from $\mathrm{Al_2O_3}$, the OFF state), the peak is less pronounced, and the coercive voltage distribution is broad. After 1000 cycles, the coercive voltage distribution in the positive polarity narrows, and the peak current increases strongly. The positive coercive voltage peak is still around 4.1 V. In the negative polarity, the coercive voltage distribution decreases, the switching peak becomes more evident, and is now located at around -3.0 V. After 2000 cycles, the switching peaks narrow further, and the peaks corresponding to positive and negative polarities are located at approximately 4.1 V and -2.7 V, respectively. The switching P-V measurement from pristine to 2000 cycles, as illustrated in Figure 5.3(b), shows an increase in remnant polarization. This increase is indicative of

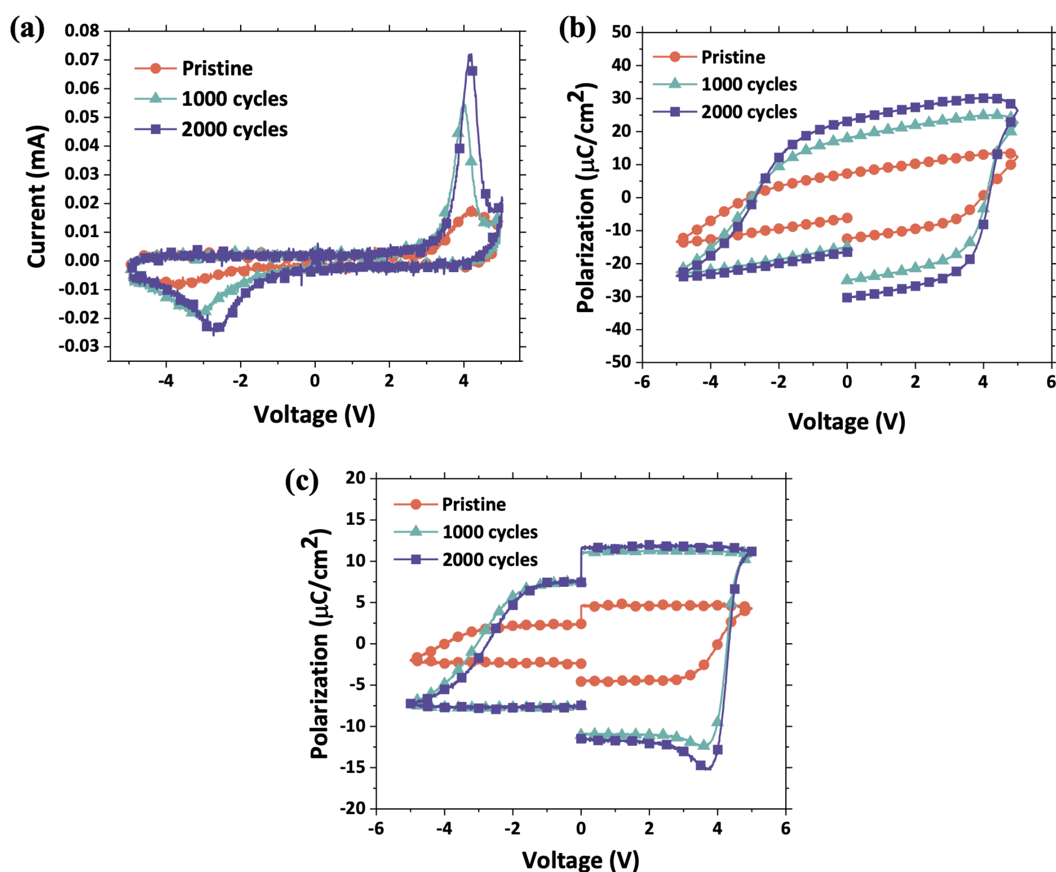

Figure 5.3: (a) I-V measurements depicting the switching behavior after the pristine state, 1000 cycles, and 2000 cycles. (b) Corresponding P-V measurements illustrating the switching characteristics for the pristine state, 1000 cycles, and 2000 cycles. (c) PUND P-V switching measurement corresponding to pristine, 1000 cycles and 2000 cycles. The wake-up cycling was executed using a square pulse with a $\pm$5V amplitude and 1 ms pulse width. The I-V and P-V measurements are performed with triangular pulse of $\pm$5V amplitude and 1 ms pulse width.

ferroelectric wake-up. From the PUND measurement shown in Figure 5.3(c), an asymmetry in the remnant polarization is observed in the positive and negative polarities noted at 11.7 $\mu\mathrm{C/cm^2}$ and -7.5 $\mu\mathrm{C/cm^2}$. As discussed in Chapter 3, this asymmetry is present in FTJ devices having dielectric layer near the bottom electrode.

Figure 5.4 shows the evolution of read currents corresponding to the Reset state (OFF state) and Set state (ON state) of the FTJ device. All measurements were conducted using the Radiant Multiferroic II tester. For the Reset operation, a square pulse with a -5.0 V amplitude and 0.5 ms pulse width was applied, while for the Set operation, a square pulse with a +5.0 V amplitude and 0.5 ms pulse width was employed. The read current corresponding to the reset and set states were measured by applying a DC voltage of +1.8

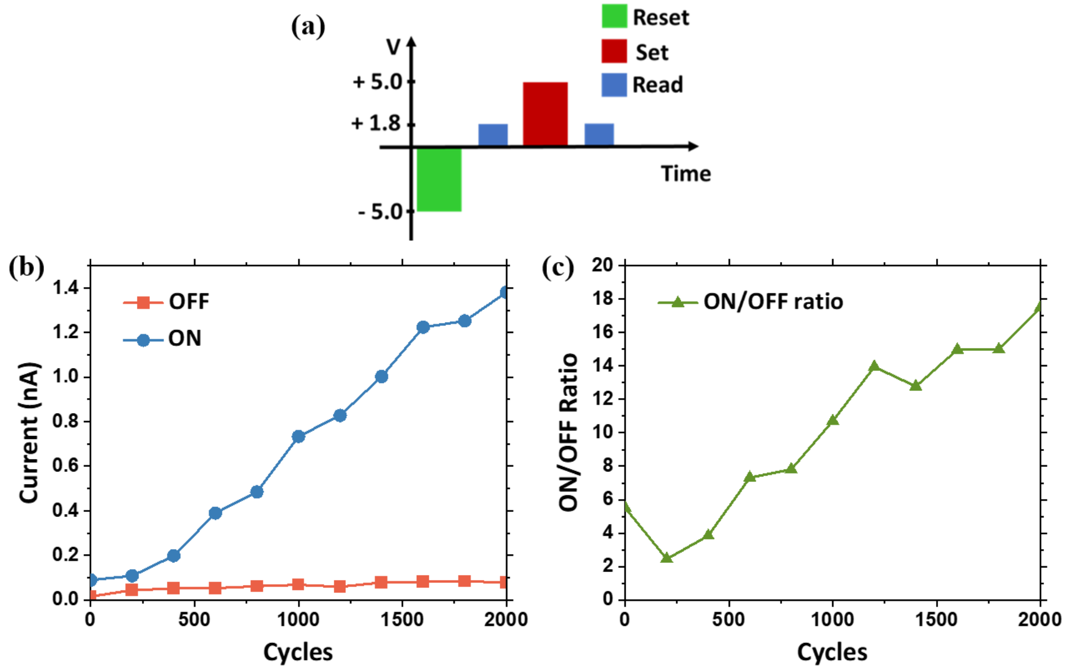

Figure 5.4: (a) Pulse sequence applied for measuring OFF and ON state currents. Reset and set procedures were executed using square pulses with amplitudes of -5.0 V and +5.0 V, respectively, and pulse widths of 0.5 ms. Read measurements were conducted utilizing a DC voltage of +1.8 V with a pulse width of 500 ms. (b) Evolution of read current associated with OFF and ON states measured under a read voltage bias with wake-up cycling. (c) Changes in the ON/OFF ratio across cycles.

V (the reported current is the average over a 500 ms measurement). The pulse sequence used for measuring the OFF and ON currents is illustrated in Figure 5.4(a). Following 2000 wake-up cycles as shown in Figure 5.4(b), the FTJ device exhibits an OFF current of approximately 0.07 nA and an ON current of about 1.38 nA. This translates to an OFF current density of 1.24 $\mu\mathrm{A/cm^2}$ and an ON current density of 24.5 $\mu\mathrm{A/cm^2}$. The evolution of the ON/OFF ratio from pristine to 2000 cycles is presented in Figure 5.4(c). In the pristine state, the ON/OFF ratio was approximately 6, and it increases to about 18 after 2000 cycles.

The FTJ device characteristics for the same W-Al_2O_3-HZO-TiN stack fabricated on the Si substrate with the same process flow used in the case of CMOS integrated FTJ device is shown in Figure 5.5 as a reference. The reference stack exhibits similar I-V switching characteristics (shown in Figure 5.5(a)) to those of the CMOS integrated device shown in Figure 5.3(a). The PUND P-V measurement shown in Figure 5.5(b) indicates a higher P_R value (in comparison to Figure 5.3(c)) of $\sim$15 $\mu\mathrm{C/cm^2}$ in the positive polarity

and ~-11 $\mu\mathrm{C/cm}^2$ in the negative polarity after 1000 cycles. This trend (as compared to Figure 5.4(b) and (c)) is also reflected on the ON, OFF currents and ON/OFF ratio of this stack as shown in Figure 5.6(c) and (d), respectively. The reference stack shows a better FTJ properties compared to the CMOS integrated FTJ device. The trend in wake-up and evolution of ON, OFF currents are similar for both the devices.

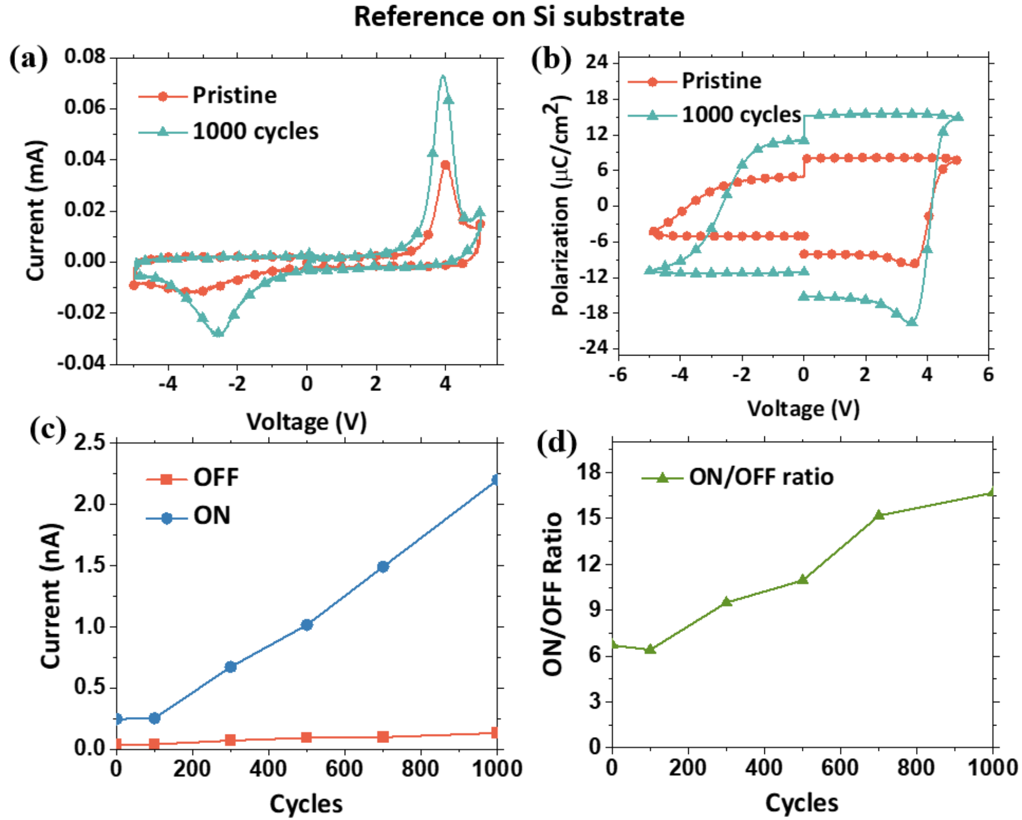

Figure 5.5: Switching (a) I-V and (b) PUND-PV measurements performed on W-Al_2O_3-HZO-TiN reference FTJ stack fabricated on Si substrate. The stack is fabricated using the same process flow employed for fabricating the FTJ device on a CMOS chip. (c) Evolution of ON and OFF currents and (d) ON/OFF ratio of the reference stack. The wake-up cycling, and measurements are performed the same way as it is done for the CMOS integrated device for a fair comparison. Here, the device area is $75 \times 75\,\mu\mathrm{m}^2$.

As discussed in Chapter 4, Reset and Set operations can be modified to attain multiple resistance states. In order to check the resistance tunability of the FTJ device integrated on the CMOS chip, potentiation/depression measurements were performed on the stand-alone FTJ device after wake-up of 2000 cycles using square pulse with ±5.0 V amplitude and a 1 ms pulse width. Figure 5.6(a) shows the pulse sequence used for attaining multiple resistance states using the voltage amplitude modification. The corresponding potentiation and depression are shown in Figure 5.6(c). Here, with the partial set opera-

tion, increasing voltage amplitude from +2.0 V to +5.0 V with pulse width of 0.5 ms, the ON current increases from 0.11 nA to 1.9 nA. Whereas with the partial reset operation, increasing voltage amplitude from -1.5 V to -5.0 V with 0.5 ms pulse width, the OFF current decreases from 1.7 nA to 0.16 nA. The range of depression (1.54 nA) is smaller than that of potentiation (1.79 nA).

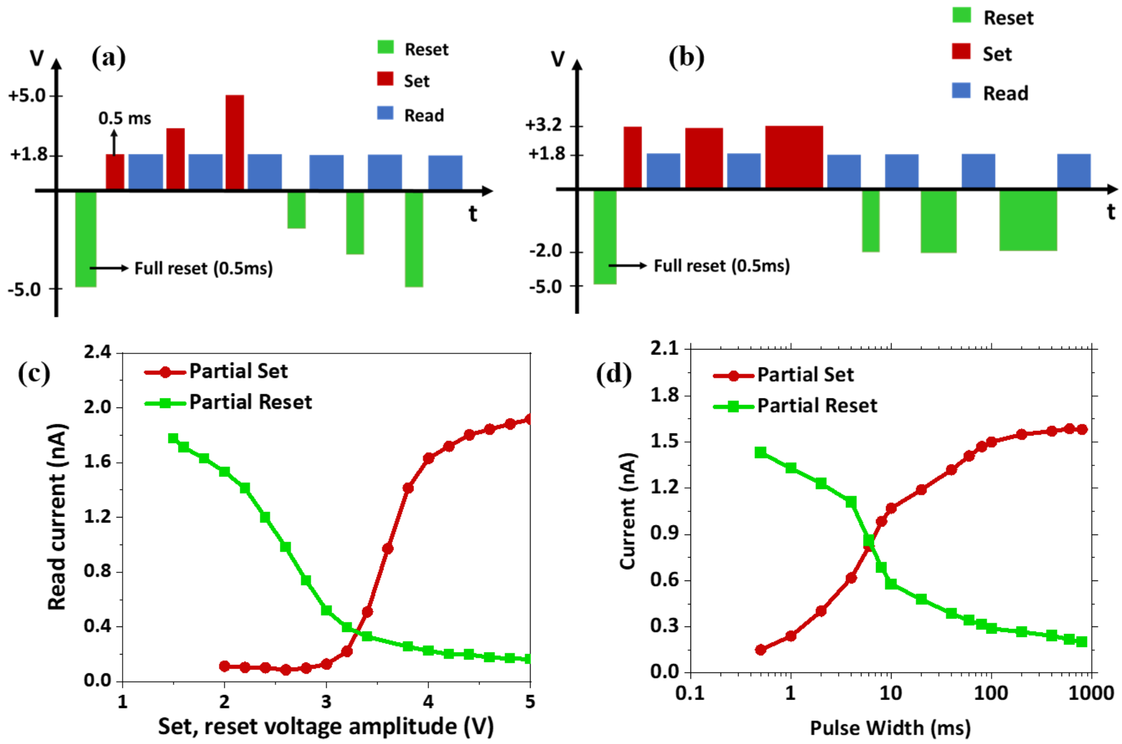

Figure 5.6: (a) Pulse sequence used for attaining multiple resistance states with voltage modification. Full reset performed with -5 V amplitude and 0.5 ms pulse width. Partial switching attained with gradual increase of set voltage amplitude from +2.0 V to +5.0 V and reset voltage amplitude from -1.5 V to -5.0 V, while keeping pulse width of 0.5 ms. (b) Pulse sequence used for attaining multiple resistance states with pulse width modification. Full reset performed with -5.0 V and 0.5 ms square pulse. Partial set voltage is set at +3.2V and partial reset voltage as -2.0 V, while increasing the set, reset pulse width from 0.5 ms to 800 ms. In both (a) and (b) read is measured with +1.8 V DC voltage application after each partial set/reset operation. (c) Potentiation and depression attained with voltage modification. (d) Potentiation and depression attained with pulse width modification.

The pulse sequence used for attaining multiple resistance states with pulse width modification is shown in Figure 5.6(b). The potentiation and depression attained with pulse width modification is shown in Figure 5.6(d). The partial set and partial reset voltages were chosen based on Figure 5.6(c), where the voltage amplitude at which partial domain switching began was selected. In the case of pulse width modification, the potentiation

leads to increase in ON current from 0.15 nA to 1.5 nA with the application of partial set pulse of +3.2 V amplitude and increasing pulse width from 0.5 ms to 800 ms. Whereas the depression leads to decrease in OFF current from 1.4 nA to 0.19 nA with the application of partial reset pulse of -2.0 V amplitude and increasing pulse width from 0.5 ms to 800 ms. In this case as well the range of depression (1.21 nA) is smaller than that of potentiation (1.35 nA). Notably, the range of potentiation and depression attained with pulse width modification is smaller than that achieved with voltage amplitude modification.

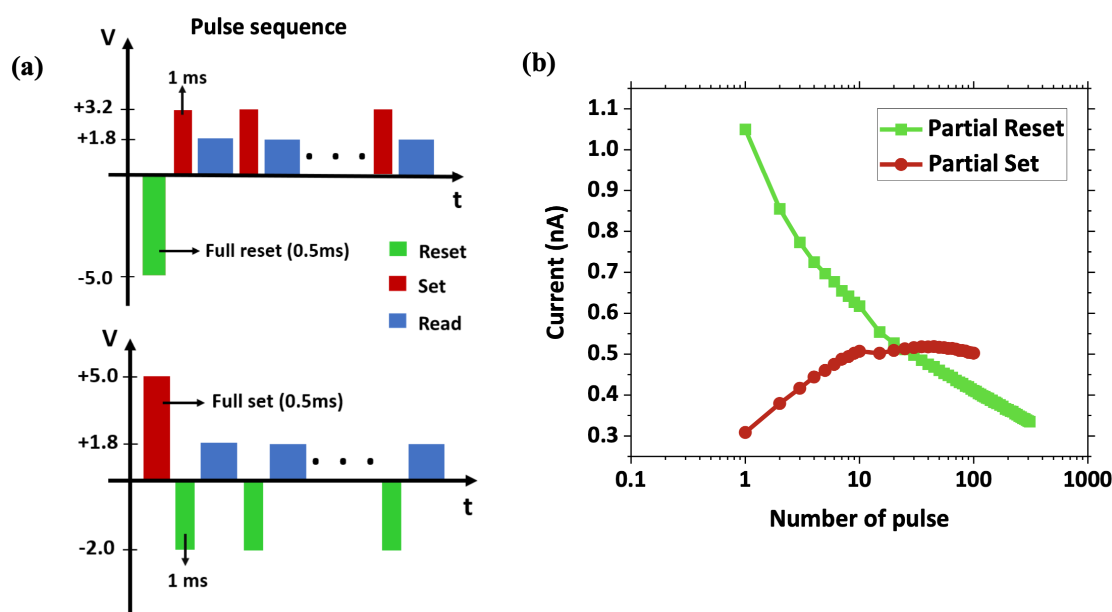

Figure 5.7: (a) Pulse sequence used for attaining multiple resistance states by applying same pulse multiple times (accumulative switching). Full reset is performed with square pulse of -5.0 V amplitude and 0.5 ms pulse width. This is followed by multiple set pulses of +3.2V amplitude and 1 ms pulse width. Whereas full set operation is performed with square pulse of +5.0 V amplitude and 0.5 ms pulse width. This is followed by multiple reset pulses of -2.0 V amplitude and 1 ms pulse width. OFF and ON state currents are measured by performing read operations after each reset and set operation with DC voltage of +1.8 V. (b) Potentiation and depression attained by applying same set, reset pulses multiple times as shown in (a).

Partial switching measurements were also performed by applying identical reset or set pulses (called accumulative switching) as shown in Figure 5.7(a). For achieving depression, the device is initially switched to ON state with a full set pulse (square, +5.0 V and 0.5 ms). This is followed by multiple partial reset operation of -2.0 V amplitude and 1 ms pulse width. However, for attaining potentiation, the device is initially switched to OFF state with a full reset operation (-5.0 V amplitude and 0.5 ms pulse width). This is

followed by multiple partial set operation of +3.2 V amplitude and 1 ms pulse width. The potentiation and depression attained by applying multiple set, reset pulses are shown in Figure 5.7(b). In case of depression the OFF current decreases from 1.05 nA to 0.33nA with 310 partial reset pulses. For potentiation, the ON current increases from 0.30 nA to 0.51 nA with 35 pulses and by applying more partial set pulse, the ON current start to decrease slightly. Accumulative switching measurements were performed on a different stack (stack C, discussed in Chapter 3), and the results were presented in Section 4.3 of Chapter 4. It was observed that, while depression could be achieved by applying multiple partial reset pulses, potentiation was not attainable in that stack. Consequently, the BEOL integrated stack (stack D, discussed in Chapter 3) appears more promising regarding resistance tunability in accumulative switching, particularly for the partial set. However, the range of potentiation (0.21 nA) is limited compared to the range of depression (0.72 nA).

5.4 Transistor measurements

During the fabrication of FTJ devices, the crystallization of HZO layer into its ferroelectric orthorhombic phase is performed at 400 °C. It is important to ensure the protection of FEOL transistors within the CMOS chip from any potential damage during this process. Transfer characteristics, typically represented by the drain current (I_D) versus gate voltage (V_G) curve, illustrate the transistor's response to variations in gate voltage, thereby demonstrating its capability to regulate the current flow between the source and drain terminals. This curve is essential in understanding the transistor's threshold voltage, saturation region, and overall switching behavior. On the other hand, output characteristics, depicted by the drain current (I_D) versus drain voltage (V_D) curve, reveal the transistor's behavior in response to variations in the drain voltage. It provides insights into saturation and triode regions, enabling a comprehensive understanding of the transistor's operational limits and efficiency.

Figure 5.8(a) and Figure 5.8(b) illustrate the transfer characteristics and output characteristics measurements of an nMOS transistor. These curves are presented to compare the transistor properties before and after the fabrication of FTJ devices on the CMOS chip. The transfer and output characteristic curves for both pre- and post-fabrication processes

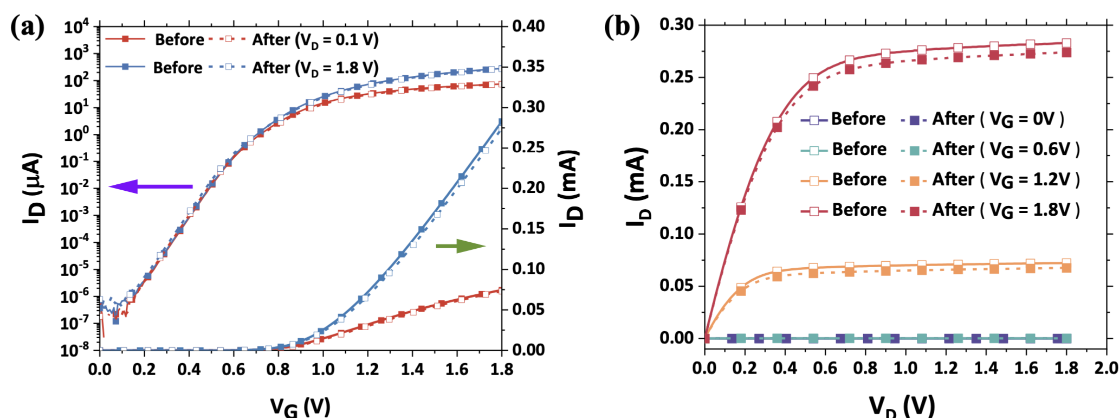

Figure 5.8: The graphs illustrate (a) the transfer characteristic (drain current (I_D) versus gate voltage (V_G)) and (b) the output characteristics (drain current (I_D) versus drain voltage (V_D)) of the nMOS transistor, both before and after the integration of FTJ devices onto the CMOS chip. This transistor is connected to the FTJ to establish a 1T1C circuit.

exhibit significant overlap, indicating that the FTJ fabrication process has not induced alterations in the transistor properties. These findings demonstrate the successful integration of the FTJ devices into CMOS BEOL without compromising the performance of the underlying transistor.

5.5 1T1C measurement to amplify FTJ output

While the FTJ device has potential for low power consumption due to voltage drive switching mechanism, the high resistance may pose a challenge in circuit implementations. It will be necessary to have higher read current which can be achieved by combining the FTJ with a nMOS transistor in common source amplifier like configuration. This is demonstrated here by connecting the bottom electrode of a FTJ with the gate of a nMOS transistor. This forms a 1T1C circuit as shown Figure 5.9(a). The 1T1C circuit, a subcircuit of 2T1C [135], allows for the amplification of the FTJ current by the connected transistor. The top and bottom electrode of FTJ which is connected to transistor also had large pad area to facilitate independent measurement of FTJ without the transistor. This is the standalone FTJ measurement as shown in Figure 5.9(b). This configuration is also employed for setting and resetting the FTJ before conducting read measurements through the transistor.

During the standalone measurement of the FTJ or to set/reset the device, the bottom

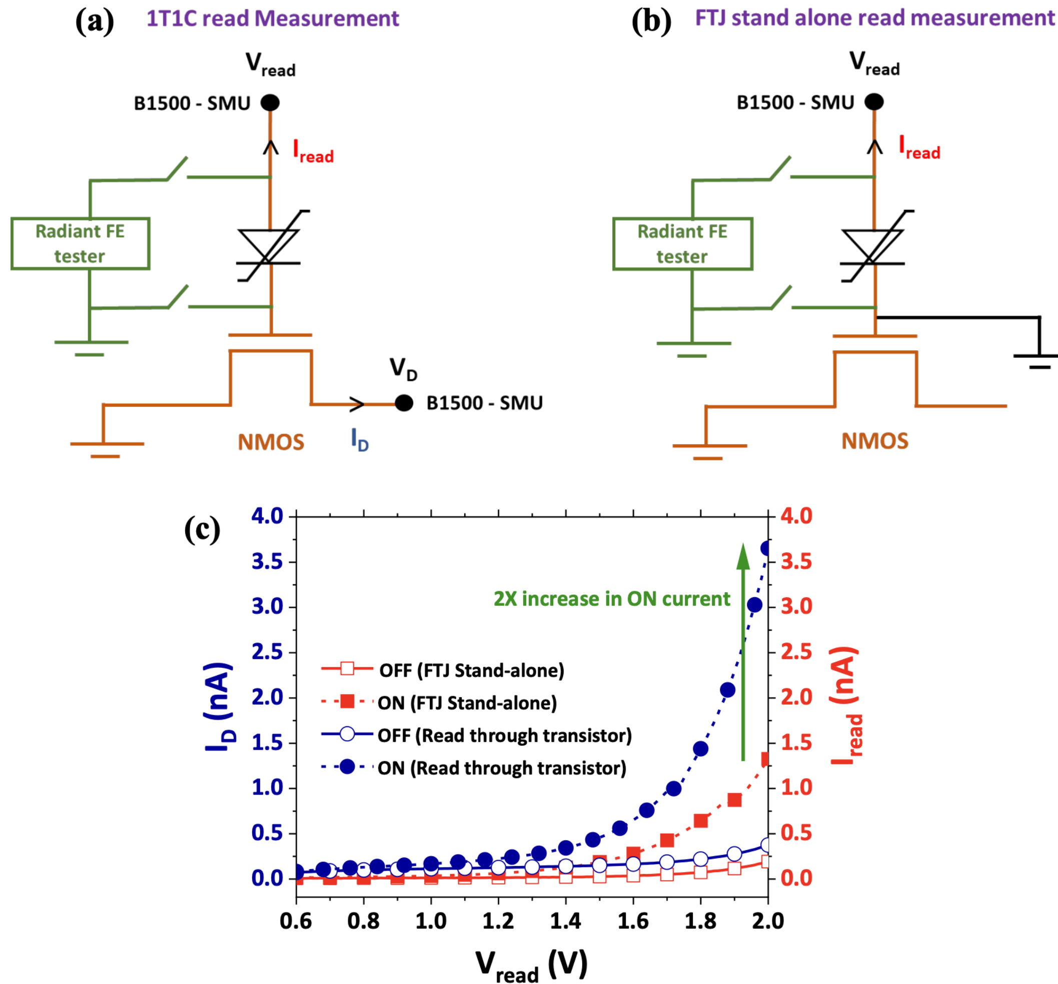

Figure 5.9: (a) 1T1C Setup schematic for amplifying the OFF and ON read currents of the FTJ device with on-chip transistor. (b) Setup schematic for measuring the OFF and ON quasi-static read current from stand-alone FTJ device (c) Graph shows the quasi-static read measurement for the stand-alone FTJ and read through the 1T1C circuit corresponding to the OFF and ON state of the FTJ device.

electrode is consistently grounded to prevent damage to the transistor. The FTJ device is switched between OFF and ON states through a reset operation (square pulse, -5.0 V, 0.5 ms) and a set operation (square pulse, +5.0 V, 0.5 ms), respectively, using the Radiant ferroelectric tester by applying voltage pulses to the FTJ top electrode. During the set or reset operation, both the source and drain of the transistor are left floating. Subsequent to the reset or set operation, the Radiant ferroelectric tester is disconnected. Once the FTJ device is either reset (OFF state) or set (ON state), the read measurement is conducted by sweeping a read voltage (V_{read}) from 0 V to 2.0 V on the FTJ top electrode. Simultaneously, a constant drain voltage (V_D) of 1.8 V is applied to the drain of the transistor, with the source terminal grounded. The measurements are conducted using the

B1500 semiconductor analyzer.

For the 180 nm CMOS technology, used in this work, the required drain voltage for the transistor is 1.8 V. As V_{read} is swept on the top electrode of the FTJ, the resulting current flowing through it charges the gate capacitor of the transistor, leading to an increase in gate-source voltage. The higher the current through the FTJ, the greater the voltage increase at the gate node of the transistor. When the FTJ is in the OFF state, the current through the device is low, resulting in a lower effective voltage on the gate. Conversely, when the FTJ is in the ON state, the current through the device is high, leading to a higher voltage at the gate node. This elevated gate-source voltage induces high current flow between the drain and source of the transistor. Given that the drain current of the transistor exponentially increases with the gate-source voltage (refer to Figure 5.8(a)), the FTJ current is effectively amplified and measured as the drain current of the transistor.

The stand-alone measurement of FTJ read current involves sweeping the top-electrode voltage from 0 V to 2.0 V while grounding the bottom electrode. In this scenario, the drain voltage (V_D) is zero (terminal not connected to B1500-SMU), and the source is not grounded. The comparison between quasi-static read currents in the OFF and ON states, measured through the FTJ-transistor (1T1C combination) and the stand-alone FTJ, is shown in Figure 5.9(c). The stand-alone measurement yields an OFF current of approximately 0.19 nA and an ON current of about 1.32 nA at a 2.0 V read voltage. The stand-alone FTJ device exhibits an OFF current density of 3.37 $\mu\mathrm{A/cm^2}$ and an ON current density of 23.4 $\mu\mathrm{A/cm^2}$, resulting in an ON/OFF ratio of $\sim$7. Following the read current measurement through the transistor, the OFF current is approximately 0.37 nA, and the ON current is around 3.65 nA at a 2.0 V read voltage. In this case, the ON/OFF ratio increased to $\sim$10, with the ON current amplified by 2.6 times. Post-amplification, the OFF current density is 6.57 $\mu\mathrm{A/cm^2}$, and the ON current density is 64.8 $\mu\mathrm{A/cm^2}$. This experiment successfully demonstrated the integration of FTJ devices on top of a CMOS chip, connected to an FEOL transistor. The observed current amplification confirms the realization of a functional FTJ-CMOS hybrid circuit, highlighting its potential for neuromorphic computing and embedded non-volatile memory applications [135,138].

5.6 Summary

In this study, we integrated W-Al_2O_3-HZO-TiN bilayer FTJ devices into the CMOS back-end-of-line and demonstrated 1T1C circuit by connecting a FTJ in the BEOL with a nMOS transistor in the front-end. DC read measurements at +1.8 V on stand-alone FTJ device yields ON/OFF ratio of 18 and ON current density of 24.5 $\mu\mathrm{A/cm^2}$. We demonstrated negligible impact on the transistor characteristics due to BEOL fabrication of the FTJ device. The 1T1C circuit was implemented to amplify the current through the FTJ and an amplification of ON current by 2.6 times was achieved. These results demonstrate the feasibility of integrating FTJ devices with CMOS technology which would be useful for neuromorphic and non-volatile memory applications.

Conclusion

The advancements in the field of ferroelectric materials facilitated the development of ferroelectric memories, which use polarization states to encode data. Although discussed as early as in 1971, the adaptation of the ferroelectric tunnel junction (FTJ) memory devices was slow due to difficulties in reducing tunnel thickness and achieving adequate read currents. The advent of epitaxial growth and atomic layer deposition (ALD) techniques eventually enabled practical demonstrations of these devices. However challenges were posed by materials like $Pb(Zr,Ti)O_3$ (PZT), $BaTiO_3$ (BTO), and $SrBi_2Ta_2O_9$ (SBT) in terms of scaling, complementary metal–oxide–semiconductor (CMOS) compatibility, and environmental safety. The discovery of an orthorhombic ferroelectric phase in Hafnium dioxide (HfO_2), a material already prevalent in the semiconductor industry, addressed many of these issues.

HfO_2-based FE memories, such as ferroelectric random access memory (FeRAM) and ferroelectric field effect transistors (FeFETs), quickly demonstrated their potential, particularly at the 28 nm technology node, showcasing better scalability compared to PZT and SBT. The low conductivity of the FTJ devices significantly reduces power consumption compared to other memristive memories. For FTJs, numerous configurations have been explored, with the metal-ferroelectric-dielectric-metal (M-FE-DE-M) stack showing particular promise due to its compatibility with Back-End-Of-Line (BEOL) processes and its ability to provide a larger memory window with a thicker ferroelectric layer of $\sim$10 nm. By 2020, substantial progress had been made with M-FE-DE-M-FTJs, particularly in developing large, cost-effective structures suitable for commercial applications. This thesis aimed to fabricate and integrate CMOS-compatible M-FE-DE-M FTJ devices into the CMOS BEOL.

The fabrication of the FTJ devices required utilization of various deposition techniques like ALD, sputtering, thermal evaporation and e-beam evaporation. The fabricated devices were evaluated and characterized with the help of electrical measurements utilizing current-voltage (I-V), polarization-voltage (P-V), positive-up-negative-down (PUND) sequence P-V, and capacitance-voltage (C-V) measurements. For attaining high performing FTJ device with high remnant polarization (P_R), high ON current, low OFF current

and high ON/OFF ratio, it is necessary to optimize the FTJ stack architecture.

In order to optimize the FTJ stack achitecture, we fabricate the M-FE-DE-M FTJ devices using Tungsten (W) and Titanium Nitride (TiN) electrodes, a Hafnuim Zirconium Oxide ($Hf_{0.5}Zr_{0.5}O_2$) ferroelectric layer, and an Aluminium Oxide (Al_2O_3) dielectric layer on a p+Si substrate at a CMOS BEOL-compatible annealing temperature of 400 $^\circ C$. Various stacks were fabricated by interchanging the dielectric and ferroelectric layers and altering the positions of the TiN and W metal electrodes. Examining the performance of these FTJ stacks provided several critical insights. The positioning of the dielectric layer and metal electrodes was found to significantly impact the FTJ performance. The W bottom electrode demonstrated optimal performance, significantly enhancing the ON/OFF ratio. This improvement is attributed to W's lower oxidation rate compared to TiN. When TiN is used as the bottom electrode, Titanium Oxide (TiO_X) forms on the bottom electrode interface, resulting in incomplete charge screening and a reduced P_R value after wake-up. Additionally, this oxide layer acts as an extra tunneling barrier, increasing the tunnel resistance in the stack with the TiN bottom electrode. Consequently, the ON current is lower in the FTJ stack with a TiN bottom electrode compared to one with a W bottom electrode. Furthermore, placing the Al_2O_3 dielectric next to the bottom electrode further enhanced the FTJ performance. This is because having the Al_2O_3 and TiO_X dielectrics in one place lead to an improved P_R value and this is also favored by the energy-band bending profile. It was also observed that charge traps at the DE-FE interface play a crucial role in the ferroelectric switching behavior where the higher concentrations of these traps stabilize larger polarization. The fabrication process, especially the annealing of the DE-FE interface, was identified as a key factor affecting charge trap density and switching behavior. Furthermore, it was determined that longer pulses are required to stabilize higher remnant polarization due to the dynamics of charge traps. The presence of charge traps are confirmed using switching and non-switching C-V measurements. And the amount of charge traps are experimentally estimated with the help of custom PUND measurement. The charge trap concentrations in 'stack anneal bottom (SAB)' and 'post anneal deposition (PAD)' stacks were quantified using device simulation, revealing a clear difference in charge trap concentration. This difference can be directly correlated to the wake-up P_R of these devices.

The study on the impact of electrical parameters on device performance highlighted the significant influence of the cycling waveform on the wake-up process and the resultant remnant polarization. In its pristine state, not all domains in the device transition from P-up to P-down when subjected to the switching voltage, due to domain pinning caused by negatively charged traps. To enable these pinned domains to switch, it is necessary to neutralize these charges through charge trapping/de-trapping or charge trap movement, processes that are more effective at higher electric fields. The higher voltage during the positive polarity phase of a 1 kHz square waveform enhances the wake-up process more than the triangular waveforms. The use of asymmetric waveforms and adjustments to pulse width increased the $\mathrm{P_R}$ after wake-up and improved the ON/OFF ratio from approximately 5 to 35. Asymmetric waveforms enabled the switching of pinned domains from the P-up to the P-down state without adding stress to domains switching from P-down to P-up, resulting in an early wake-up. Modifying the pulse width of the wake-up pulse scheme from pristine to 1000 cycles delayed fatigue, leading to an improved ON/OFF ratio of 35 after 1000 cycles. In this work, we demonstrated that optimizing the wake-up operation is as crucial as optimizing the device architecture to achieve optimal performance in bilayer FTJ devices.

The ability to switch the conductance of FTJ devices in an analog manner is essential for their use in neuromorphic applications. In this work, we achieved multiple resistance states in the FTJ device by modifying the Reset and Set pulses. Techniques such as adjusting the Reset/Set voltage amplitude or pulse width, and employing accumulative switching by repeatedly applying the same pulse were demonstrated on the FTJ stacks to achieve multiple resistance states. This study showed that the opimized FTJ device holds significant potential for use in neuromorphic hardware systems.

Finally, an optimized bilayer FTJ stack with W bottom electrode and TiN top electrode with Al_2O_3 positioned near the bottom electrode is successfully integrated to the BEOL of CMOS wafer. Standalone FTJ devices in the BEOL exhibited an ON/OFF ratio of 18 and an ON current density of 24.5 $\mu\mathrm{A/cm^2}$. Importantly, the BEOL fabrication process had a negligible impact on the characteristics of front-end-of-line (FEOL) transistors. Additionally, a 1 transistor-1 capacitor (1T1C) circuit was utilized by connecting a standalone FTJ device to the FEOL transistor. This connection amplified the ON current

by 2.6 times leading to an ON current density of 64.8 $\mu\mathrm{A}/\mathrm{cm}^2$. This work demonstrated the practicality and potential of FTJ-CMOS integration for neuromorphic computing and non-volatile memory applications.

These FTJ devices exhibit non-ideal neuromorphic behaviors, such as nonlinearity in the various resistance states achieved through the partial switching of domains. This can be addressed through circuit designs. This work serves as a preliminary milestone in establishing FTJ devices as a commercial memory technology for neuromorphic applications. For practical use, the FTJ devices discussed in this thesis need to be scaled down and multiple FTJ devices needs to be integrated as arrays within the relevant circuit locations. To enhance the reliability of these devices, a statistical study must be conducted to understand device-to-device variability. This variability can be minimized by optimizing the individual deposition and fabrication techniques, thereby ensuring consistent device quality across the entire CMOS wafer. Recognizing the importance of charge traps at the FE-DE interface for FTJ device functionality, alternative techniques for interface engineering must be explored to optimize charge concentrations and enhance FTJ device performance. New methods must be developed to maintain ferroelectric properties at nanometer scales, facilitating the high-density integration of FTJ devices. Investigating polarization switching dynamics at the atomic level will help to enhance the switching speeds. Further research is needed to improve the endurance and retention characteristics of ferroelectric materials for long-term reliability. Additionally, the thermal stability of M-FE-DE-M FTJ devices and their behavior under varying environmental conditions must be studied.

Although M-FE-DE-M FTJ devices have been thoroughly studied for stack and performance optimization and have shown compatibility with CMOS BEOL, further research is necessary for commercialization. This involves developing cost-effective fabrication processes, conducting cost-benefit analyses, establishing standardized testing protocols, and collaborating with industry stakeholders to set performance and reliability standards.

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List of Publications

1. **Keerthana Shajil Nair**, Marco Holzer, Catherine Dubourdieu, and Veeresh Deshpande. Cycling waveform dependent wake-up and ON/OFF ratio in Al_2O_3 / $Hf_{0.5}Zr_{0.5}O_2$ ferroelectric tunnel junction devices. *ACS Applied Electronic Materials*, 5(3) : 1478–1488, 2023.

2. Riccardo Fontanini, Mattia Segatto, **Keerthana Shajil Nair**, Marco Holzer, Francesco Driussi, I Hausler, C T Koch, C Dubourdieu, V Deshpande, and D Esseni. Charge-trapping-induced compensation of the ferroelectric polarization in FTJs: Optimal conditions for a synaptic device operation. *IEEE Transactions on Electron Devices*, 69(7):3694–3699, 2022.

3. Veeresh Deshpande, **Keerthana Shajil Nair**, Marco Holzer, Sourish Banerjee, and Catherine Dubourdieu. CMOS back-end-of-line compatible ferroelectric tunnel junction devices. *Solid-State Electronics*, 186:108054, 2021.

List of Abbreviations

AFE	Antiferroelectric
ALD	Atomic layer deposition
ANN	Artificial neural networks
BEOL	Back-end-of-line
CMOS	Complementary metal-oxide-semiconductor
CPU	Central processing units
CVD	Chemical vapor deposition
DC	Direct current
DE	Dielectric
DRAM	Dynamic random access memory
DT	Direct tunnelling
DUT	Device under test
FE	Ferroelectric
FeFET	Ferroelectric field effect transistor
FeRAM	Ferroelectric random access memory
FNT	Fowler-Nordheim tunnelling
FTJ	Ferroelectric tunnel junction
GIXRD	Grazing incidence X-ray diffraction
GPC	Growth per cycle
HAXPES	X-ray photoelectron spectroscpy
HRS	High resistance state
HZO	$Hf_{0.5}Zr_{0.5}O_2$
IoT	Internet of things
KAI	Kolmogorov-Avrami-Ishibashi model
LIF	Leaky-integrate-and-fire neuron model
LRS	Low resistance state
LTD	Long-term depression
LTP	Long-term potentiation
NLS	Nucleation-limited switching model
PCM	Phase change memories

PUND	Positive-Up-Negative-Down
PVD	Physical vapour deposition
PZT	Lead Zirconate Titanate
RIE	Reactive ion etching
RTP	Rapid thermal processing
SNN	Spiking neural networks
SRAM	Static random access memory
STD	Short-term depression
STDP	Spike-Timing-Dependent Plasticity
STP	Short-term potentiation
TEMAH	Tetrakys-ethyl-methyl-amino hafnium
TEMAZ	Tetrakys-ethyl-methyl-amino zirconium
TER	Tunnelling electroresistance
XPS	X-ray photoelectron spectroscopy
XRD	X-ray diffraction