Electronic Synapses Enabled by an Epitaxial SrTiO$_{3-\delta}$ / Hf$_{0.5}$Zr$_{0.5}$O$_2$ Ferroelectric Field-Effect Memristor Integrated on Silicon

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Synapses play a vital role in information processing, learning, and memory formation in the brain. By emulating the behavior of biological synapses, electronic synaptic devices hold the promise of enabling high-performance, energy-efficient, and scalable neuromorphic computing. Ferroelectric memristive devices integrate the characteristics of both ferroelectric and memristive materials and present a far-reaching potential as artificial synapses. Here, it is reported on a new ferroelectric device on silicon, a field-effect memristor, consisting of an epitaxial ultrathin ferroelectric Hf$_{0.5}$Zr$_{0.5}$O$_2$ film sandwiched between an epitaxial highly doped oxide semiconductor SrTiO$_{3-\delta}$ and a top metal. Upon a low voltage of less than 2 V, the field-effect modulation in the semiconductor enables to access multiple states. The device works in a large time domain ranging from milliseconds down to tens of nanoseconds. By gradually switching the polarization by identical pulses, the ferroelectric diode devices can dynamically adjust the synaptic strength to mimic short- and long-term memory plasticity. Ionic contributions due to redox processes in the oxide semiconductor beneficially influence the device operation and retention.

1. Introduction

A long-term goal of the research and engineering community is to resolve the issue of handling a large variety of inhomogeneous, unstructured, and noisy data with energy efficiency that rivals that of the human brain by adopting in-memory or brain-inspired neuromorphic computing.[1] Emerging non-volatile memories (NVMs) with memristive properties such as metal oxide resistive random-access memory (OxRAM), phase change memory (PCM) or conductive bridge RAM (CBRAM) are good candidates to implement in-memory computing in hardware.[2] In contrast to the aforementioned NVMs, which are current-driven, ferroelectric NVMs are voltage-driven and therefore offer the potential for developing low to ultra-low power computing platforms.[3] Among the three main ferroelectric types of memories[4]-

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ferroelectric RAM (FeRAM), ferroelectric tunnel junction (FTJ) and ferroelectric field-effect transistor (FeFET) – the FTJ is particularly attractive since it is a simple two-terminal device consisting of a metal/ferroelectric/metal stack that has a non-destructive readout. The operation of FTJs[5] relies on the modulation of the tunnel barrier, hence of the tunneling current or the conductance, by the ferroelectric polarization due to an asymmetric compensation of polarization charges at the two electrodes. Progressive switching of ferroelectric domains controlled by a voltage leads to partial polarization and, hence, to multiple conductance states making the FTJ function as a memristor. The first FTJ ferroelectric memristor has been demonstrated using the perovskite ferroelectrics $BaTiO_3$[6,7] and synaptic behavior was later demonstrated with $BiFeO_3$.[8] By combining perovskite FTJs with bulk Nb-doped $SrTiO_3$ semiconductor bottom electrode[9,10] and taking advantage of ferroionic effects,[11,12] giant tunneling electroresistances (TERs) up to 10^7 have been obtained.[13]

HfO_2-based fluorite ferroelectrics are much more attractive than perovskite materials for FTJs as they exhibit robust ferroelectricity down to a few nanometers and they are fully compatible with complementary metal oxide semiconductor (CMOS), which is a huge advantage.[14,15] However, the requirement for ultrathin (<5 nm) $Hf_{0.5}Zr_{0.5}O_2$ (HZO) is a big obstacle. Indeed, with few exceptions[16,17] ferroelectricity in thin HZO becomes metastable[18] or totally unstable below 5 nm due to a large depolarization field, hampering the fabrication of functional FTJs. On the other hand, thicker HZO near 10 nm brings the device out of the direct tunneling regime and leads to unfavorably high programming voltages[19] and a rather high energy consumption of up to 1.8 pJ per programming event. The latter is comparable to OxRAM but considerably larger than biological synapses (1 to 10 fJ) .[20] In a different design, composite double-layer (e.g., HZO/Al_2O_3) FTJs with a thick HZO film (typically 10 nm) have been proposed showing good tunneling Electroresistance (TER) and synaptic plasticity,[21–26] however, at the expense of an increased programing voltage of typically ≈ 5 V and a significant retention loss, presumably caused by excess depolarization fields induced by the (Al_2O_3) dielectric. Hence, functional synaptic devices with a single thin layer of HZO (≈5 nm), are highly desirable to achieve improved reliability and low programming voltages compatible with current CMOS technologies.

The ferroelectric field effect diode which we propose in this work has the potential to break new grounds. In contrast to a typical HZO FTJ, the bottom electrode is not a metal but a doped oxide semiconductor with a key active role in the device operation. In brief, partial polarization switching in HZO induces a field effect in the semiconductor, which should favor the ability to set up multiple non-volatile resistance states. Setting the HZO thickness at an optimum value of ≈5 nm, we ensure a robust ferroelectricity and therefore low voltage operation but also a small write current, which is expected to result in a low energy consumption per programming event. Devices of this kind have been realized using a thin tunable resistive WO_{3-x} electrode, which show promising synaptic behavior.[27,28] However, employing a semiconducting oxide electrode such as doped $SrTiO_{3-\delta}$ as bottom electrode has the potential to bring new avenues over resistive metallic oxides. $SrTiO_{3-\delta}$ can be grown epitaxially on silicon and may thus offer the ability to realize a fully epitaxial $HZO/SrTiO_{3-\delta}$ based ferroelectric memristor on silicon. Compared to the widely studied polycrystalline HZO, epitaxial HZO is expected to host a larger and more homogeneous ferroelectric polarization especially for ultrathin films. Moreover, ferroelectric switching and domain propagation in epitaxial HZO are expected to be less restricted by high-angle grain boundaries, which could significantly influence the synaptic behavior of the devices. Finally, the strong ionicity and redox reactions[29] associated with oxygen vacancies inherent to $SrTiO_{3-\delta}$ provides an additional key knob to achieve device performance at larger time scales similar to those found in biological synapses.

In this work, we demonstrate an HZO-based ferroelectric field effect memristor in the metal/ferroelectric/semiconductor configuration with a thin epitaxial HZO of ≈5 nm, which exhibits synaptic plasticity such as symmetric potentiation/depression remarkably achieved with identical pulses, pair pulse facilitation, and spike timing dependent plasticity in several time scales ranging from tens of ns to ms. We show that the operation with identical pulses is a direct consequence of time voltage tradeoff, which is a unique property of fluorite ferroelectrics in the investigated time scales. The key component in our design is an ultrathin (10-20 nm) n-type $SrTiO_{3-\delta}$ semiconductor layer used as bottom electrode, epitaxially grown on Si(001). This layer does not only function as a simple electrode but it has a multifunctional active role. It allows the epitaxial growth of orthorhombic HZO by means of domain-matching epitaxy. It also provides not only the necessary asymmetry for the device operation but also enforces the non-volatile modulation of the device conductance by the field-effect of the ferroelectric. The ionic motion of the oxygen vacancies deliberately introduced in the epitaxial $SrTiO_{3-\delta}$, benefits the dynamic range of the synapses during potentiation and depression at time scales of more than 50 μs and to their retention behavior. These electronic synapses operate at a low voltage of 2 V or below and with an ultralow energy consumption per programming event of ~ 8 fJ, which rivals biological synapses.

2. Results

The results presented here are obtained from samples of HZO grown on epi-$SrTiO_{3-\delta}$/Si substrates and are compared with reference samples of HZO grown on commercially available bulk Nb (0.7 at.%): $SrTiO_3$ substrates. The details of the molecular beam epitaxy (MBE) growth for both HZO and epi-$SrTiO_{3-\delta}$ on Si(001) substrates are given in the Methods section as well as the details for the top electrode and device fabrication. The epi-$SrTiO_{3-\delta}$ is deliberately prepared oxygen deficient during the MBE growth so that oxygen vacancy donors make $SrTiO_{3-\delta}$ a heavily n-type doped semiconductor, as required to function as a bottom electrode. The atomic concentration of oxygen vacancies (0.56 at. %) and associated electron carrier concentration (5.3-5.7 $\times10^{20}$ cm^{-3}) were estimated by X-ray photoelectron spectroscopy (XPS) (Figure S1a, Supporting Information) and details are given in the Supplementary note 1. Moreover, from current driven 4-point probe measurements (Figure S1b, Supporting Information) on 10 nm $SrTiO_{3-\delta}$ on insulating Si substrate, the $SrTiO_{3-\delta}$ resistivity was found to be $\rho = 0.023$ Ω.cm indicative of a doped layer. The $SrTiO_{3-\delta}$ /Si samples were kept under vacuum until they were capped with HZO, so the influence of environmental conditions is considered to be minimal. Any possible ion movement in the $SrTiO_{3-\delta}$ due to interaction with the environment is expected to

equilibrate and stabilize during the time of few days that elapsed between the device fabrication and the electrical measurement experiments. Therefore, no influence of the air exposure on the electrical measurements, retention measurements in specific is expected.

2.1. Epitaxial HZO/SrTiO$_{3-\delta}$ on Silicon

X-ray diffraction (XRD) performed on the SrTiO$_{3-\delta}$ films deposited on Si shows the single crystalline nature of the perovskite, of which unit cell is rotated by 45° relatively to the Si one, with the following epitaxial relationship: $(001)_{STO} \parallel (001)_{Si}$ and $[100]_{STO} \parallel [110]_{Si}$ (Figures S2a,b, Supporting Information). The X-ray reflectometry (XRR) pattern of the 10 nm SrTiO$_{3-\delta}$ / 5 nm HZO stack is shown in Figure S2c, Supporting Information. It proves smooth interfaces with rms roughness well below 1 nm. The individual film thicknesses were determined as $t_{STO} = 10.1 \pm 0.5$ nm and $t_{HZO} = 4.7 \pm 0.5$ nm. The single crystalline nature of HZO is derived from the pole figures performed on the 111 and 200/020/002 Bragg reflections of HZO shown in **Figures 1**a,b, respectively. Besides the sharp peaks originating from Si 111 (marked by small white circles), comparatively broader ones caused by the HZO film are observed. A detailed analysis, assuming the lattice parameters of a pure orthorhombic phase, shows that excellent agreement between modeling (large circles) and experiment is obtained when the following assumptions are made: first, the epitaxial relationships are <121>HZO $\parallel$ <100> SrTiO$_{3-\delta}$ $\parallel$ <110>Si and <1̄01>HZO $\parallel$ <010> SrTiO$_{3-\delta}$ $\parallel$ <1̄10>Si, second the HZO (111) planes are tilted by about 14° from the surface normal towards the <100> SrTiO$_{3-\delta}$ $\parallel$ <110>Si direction.

Both pole figures exhibit fourfold in-plane symmetry caused by the fourfold symmetry of the underlying SrTiO$_{3-\delta}$/Si (001) substrate which is supported by the simulations. This demonstrates that the HZO film is epitaxially grown on the SrTiO$_{3-\delta}$ layer and exhibits domains that differ in their azimuthal orientations at steps of 90° angles.

The epitaxial relationship determined from the XRD pole figure analyses is further confirmed by High Resolution Transmission Electron Microscopy (HRTEM) at the local nm scale. A representative HRTEM cross-section of the stack and a detail of the HZO with superimposed modeling schematic and simulated HRTEM image are shown in Figure 1c,d, respectively. The atomic structural model, which is overlapped in Figure 1d, of the HZO structure was simulated with VESTA in the [10$\bar{1}$] orientation. The simulated HRTEM image was obtained assuming an orthorhombic structure of HZO with space group Pca2$_1$, at the experimental conditions of defocus -30 nm and a specimen thickness of 40 nm and was extracted from Figure S3c. A corresponding simulated image assuming tetragonal phase (Figure S3d) did not yield good matching for the given experimental conditions, indicating that the observed crystallite has the orthorhombic structure. From the HRTEM analysis we can conclude that HZO has a ferroelectric orthorhombic structure. The fast Fourier transform (FFT) in Figure 1e shows the HZO and STO peak indexing, in compatibility with [10$\bar{1}$]$_{HZO}$ zone axis $\parallel$ [010]$_{STO}$. By filtering all peaks except the circled 020$_{HZO}$ and 200$_{STO}$ ones, the lattice fringes image in Figure 1f is obtained indicating a near coincidence lattice[30] or

domain matching epitaxy (DME)[31] in such a way that 4 (3) lattice planes of HZO match with 5 (4) lattice planes of SrTiO$_{3-\delta}$, accompanied by the formation of geometrical dislocations. The domain matching epitaxy results in an effective lattice mismatch between HZO and SrTiO$_{3-\delta}$ of −1.64% along [010]$_{STO}$, which is much smaller than the lattice mismatch of −26.23% obtained for bulk HZO and SrTiO$_3$ on the basis of their lattice parameter difference along the same direction. Details of the calculations can be found in Note S3, Supporting Information. The domain matching epitaxy with the favorable lattice mismatch observed at a local scale by HRTEM (Figure 1f) could be considered as the driving force for the epitaxial growth on cm-scale specimens observed by XRD (Figure 1a,b).

Our structural data agree with those previously published on epitaxial HZO on Nb:SrTiO$_3$ substrate, with four (111) domains misoriented from the surface normal by 15°.[32] In this latter work, however, no ferroelectricity was reported. Epitaxial Si-doped HfO$_2$ on Nb:SrTiO$_3$ (001) with a [002] orientation perpendicularly to the substrate has been reported.[33] The films were ferroelectric but memristive behavior and synaptic plasticity were not addressed.[33] It should be noted that most of the work on the epitaxy of HZO is performed on a La$_{0.7}$Sr$_{0.3}$MnO$_3$ (LSMO) metal oxide template on SrTiO$_3$/Si substrates or on bulk oxide substrates (e.g., on scandates).[34–37] Our work is, to the best of our knowledge, the first demonstration of ferroelectric HZO epitaxially grown directly on SrTiO$_{3-\delta}$-buffered Si (100).

In the next sections, we demonstrate that our epitaxial HZO/SrTiO$_{3-\delta}$ devices on silicon are not only ferroelectric but that they can emulate the function of synapses with a large variety of synaptic plasticity.

2.2. Ferroelectricity and Memory Characteristics

The P-V and displacement current I-V characteristics of epitaxial devices (area 50×50 μm^2) measured at 1 kHz in the pristine and wake-up states are given in **Figure 2**a,b. Despite the small HZO thickness (∼ 5 nm), a relatively large remanent polarization P_r ∼14 μC/cm^2 is obtained (from positive up, negative down (PUND) measurements – see Figure S4, Supporting Information). The coercive voltage V_c is small, around 1 V, which suggests that the memory devices can be programmed at a rather low voltage of less than 2 V. Similar hysteresis characteristics are found for the reference devices fabricated on bulk Nb:SrTiO$_3$ as shown in Figure S5, Supporting Information. The P-V and field cycling ("wake-up") characteristics are similar to those previously obtained on Ge substrates[18] for the same HZO layer thickness. A frequency dependence of the P-V loops is observed (see Figure S6) where the coercive field E_c (voltage V_c) increases with frequency f as $E_c = f^\beta$, with $\beta \sim 0.23$ in agreement with theory[38] mainly applying to epitaxial or single crystal ferroelectrics.

At lower frequencies (< 1 kHz), a small increase of P_r is observed in the P-V measurements (Figure S6a, Supporting Information), which may affect the response of the devices at large time scales (> 1 ms). This increase was also reported in bilayer HZO/Al$_2$O$_3$ FTJs[25] and is associated to charging or discharging of traps near the ferroelectric-dielectric interface, which happens over longer pulse times, allowing a higher polarization to be stabilized.
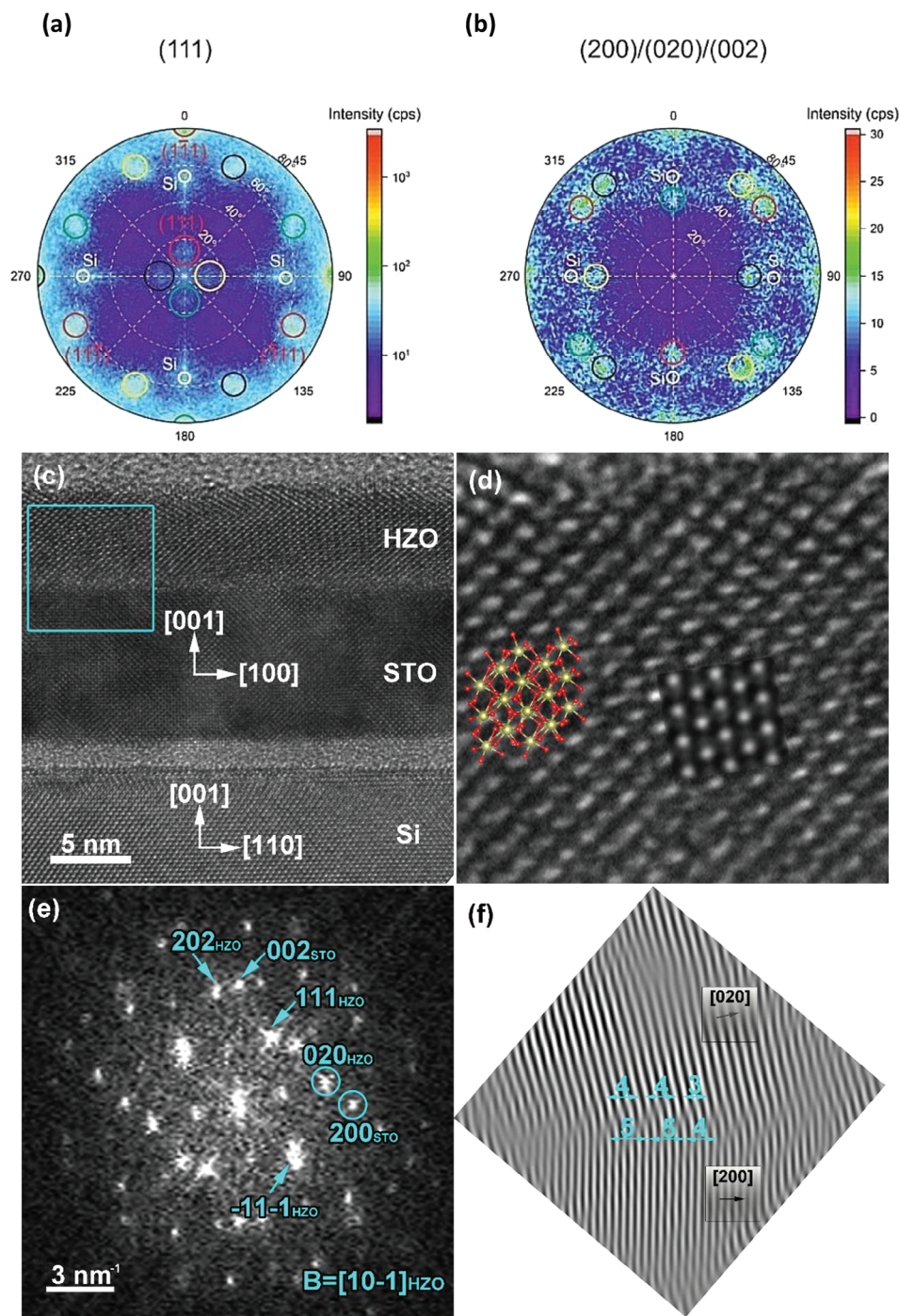
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Figure 1. Structural characterization of epitaxial 5 nm $Hf_{0.5}Zr_{0.5}O_2$ (HZO) on epitaxial 10 nm $SrTiO_{3-\delta}$ on Si (001). X-ray pole figures performed a) on the HZO 111 Bragg reflection at $2\theta = 30.25°$, and b) on the HZO 200/020/002 Bragg reflections at $2\theta = 35.00°$. The small white circles mark the Si {111} family planes. The colored open circles show simulated positions of ${111}_{HZO}$ family planes, which are inclined by about 14° with respect to the Si (001) substrate. The inclination points towards the <100> $SrTiO_{3-\delta}$ / <110>Si direction. Different colors – red, black, green, and yellow – indicate 0°, 90°, 180°, and 270° rotated in-plane variants, respectively. c) High Resolution Transmission Electron Microscopy (HRTEM) cross-section image of the stack, d) magnified view of an HZO crystallite in which the atomic structural model of the orthorhombic phase HZO in the $[10\bar{1}]$ zone axis was superimposed together with the simulated HRTEM image at a defocus of −30 nm and a thickness of 40 nm, e) Fast Fourier Transform (FFT) pattern performed on an area marked by the blue square in c) which contains both the HZO and STO thin films, together with another FFT pattern (top left of the image) obtained from an HZO crystallite viewed along $[10\bar{1}]$ zone axis, f) Fourier-filtered micrograph obtained using $(020)_{HZO}$ and $(200)_{STO}$ as indexed in the FFT picture in e).
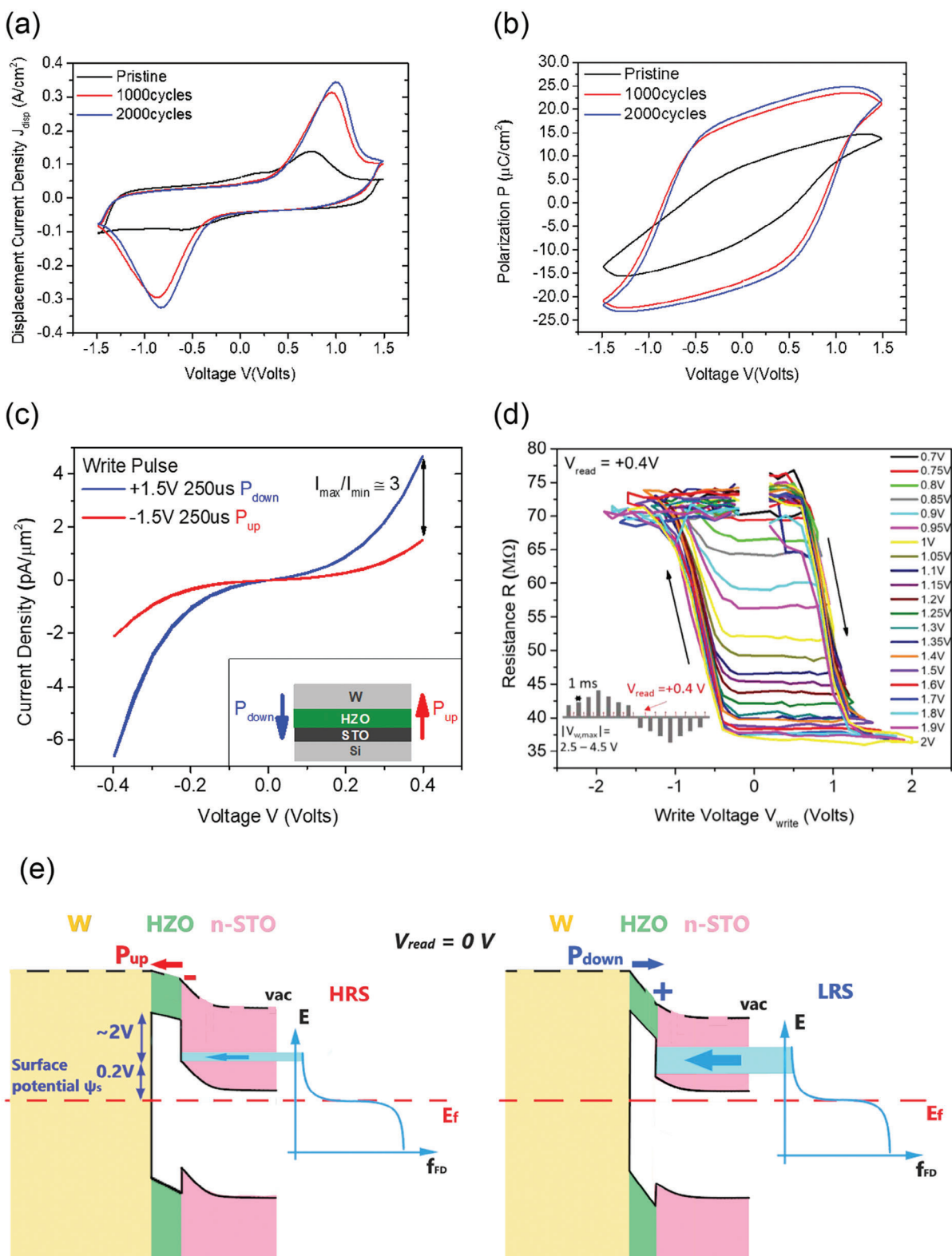
Figure 2. Ferroelectric characteristics and multiple resistance states of W/HZO/SrTiO$_{3-\delta}$/Si memristive device. a), b) Displacement current and polarization as a function of applied voltage at 1 kHz. c) I-V characteristic for two different polarization states of the ferroelectric film. d) Resistance measurement of the memristive device using pulses with variable pulse amplitude (inset) in the range 0.7–2.0 V, showing a large number of intermediate states. V$_{read}$ (+0.4 V) is the voltage used to measure the current through the HZO and hence the resistance. e) Band diagrams showing the modulation of the surface potential Ψ$_s$ by the polarization P in the high (HRS) and low (LRS) resistance states. f$_D$ denotes the Fermi-Dirac distribution.

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The I-V characteristics in the P_{UP} and P_{DOWN} states are shown in Figure 2c. At a read voltage $V_{read} = +0.4$ V, the I_{ON}/I_{OFF} ratio is 3 while the I_{ON} ranges between 0.1 and 1 pA μm^{-2}. These values are similar to those obtained on bilayer stack FTJs[23,26]. The low I_{ON} is expected since the tunneling barrier HZO is relatively thick (5 nm) and the HZO barrier rather high (≈2 eV)[39], making it difficult to obtain high direct tunneling current[4,5].

To obtain the resistance memory loops (shown in Figure 2d) the devices were programmed using a sequence of 1 ms square voltage pulses of different amplitudes (see inset of Figure 2d) and the current passing through the ferroelectric was measured at a fixed read voltage $V_{read} = +0.4$ V. The resistance was then extracted as $R = V_{read}/I$ and is plotted in Figure 2d. The dynamic range defined by the ratio of maximum to minimum resistances is around 200%. More than 16 stable intermediate nonvolatile states can be accessed, with good sense margin, which corresponds to a 4-bit memory. The resistance change occurs at around 1 V, which is in line with the coercive voltage of the P-V loops (Figure 2a,b), indicating that the resistance memory loop (Figure 2d) is associated with the ferroelectric switching. Programming the thin HZO memristive devices at a low voltage of ≈1.5–2 V is compatible with voltage scaling of current CMOS and shows significant advantage over the bilayer FTJs, which operate at higher voltages (≈4–5 V).[23,26]

To get a deeper understanding of the electroresistance mechanism, the I-V curves were measured at different temperatures (Figure S7, Supporting Information) and analyzed assuming Schottky emission which yields a potential barrier Φ_B of 0.2 eV for thermionic emission. This value of Φ_B is about an order of magnitude smaller compared to that of the HZO barrier of about 2 eV[39] formed due to the conduction band offsets between the metal electrodes and HZO. It is anticipated that the relevant barrier of 0.2 eV corresponds to the surface potential Ψ_s at the HZO/n-SrTiO$_{3-\delta}$ interface. Ψ_s can have a finite value even at $V = 0$ because of the finite workfunction difference between the top metal electrode and the bottom SrTiO$_{3-\delta}$ semiconductor. Moreover, Ψ_s can be modulated by the gate voltage V and the polarization P. In the P_{DOWN} polarization state, the positive polarization bound charges lower the electron potential at the HZO/ SrTiO$_{3-\delta}$ interface, thus lowering or diminishing Ψ_s. This allows a large number of carriers to pass through the HZO barrier and give rise to a high I_{ON} current or low resistance. On the contrary, in the P_{UP} state, the negative polarization bound charges raise the electron potential at the interface, consequently raises Ψ_s. In this case, Ψ_s forms a high and wide barrier that filters low energy electrons, allowing only a small population of carriers as determined from the tail of the Fermi Dirac distribution with energies higher than Ψ_s to pass through HZO yielding a low I_{OFF} current or high resistance. In a different but fully equivalent interpretation we could say that the applied bias and the associated polarization bound charges change the electron population of the semiconductor near the interface, hence its resistance. For the P_{UP} polarization the semiconductor is depleted increasing the total resistance of the junction (left panel of Figure 2e). For P_{DOWN} polarization the electron population of the semiconductor is larger near the interface, thus reducing the total junction resistance (right panel of Figure 2e). Therefore, the mechanism giving rise to the electroresistance is thought to be a field effect modulation of the surface potential or, equivalently, the resistance of the semiconduc-

tor near the interface, mediated by the polarization in the HZO that gives this effect a non-volatile character. It should be noted that the current could have a small direct quantum mechanical tunneling component modulated by the HZO barrier through P as in an FTJ, but it is not necessary. Any transport mechanism giving rise to small leakage currents through HZO would be acceptable since the change in electro-resistance originates from the modulation of Ψ_s in the semiconductor independent of the transport mechanism through the HZO.

2.3. Retention

The retention measurements at room temperature (RT) and 85 °C are given in Figure. 3a,b, respectively, and are compared to those at RT of a memristive device with a bulk Nb:SrTiO$_3$ as the bottom electrode (**Figure 3**c). No retention loss for times up to 10^4 s is observed in the latter case. In contrast, the HZO memristors on epi-SrTiO$_{3-\delta}$ on silicon (Figure 3b) show a distinctly different behavior: while the written low resistance state (LRS) at RT exhibits a very good retention with only a slight drift towards higher resistance, the high resistance state (HRS) shows a pronounced drift towards higher resistances after about 1000 s. The intermediate states lying closer to the LRS mimic the behavior of the latter states but with a slightly larger drift to higher resistance while those lying closer to the HRS exhibit a much stronger drift towards high resistance mimicking the HRS behavior. The same trend is observed at 85 °C (Figure 3c) with a more pronounced increase of the intermediate and HRS states toward higher resistance. These observations are counter-intuitive because the drift of HRS to higher resistance is unexpected and leads to an increasing memory window in the course of time contrary to most ferroelectric memristive devices, which show the opposite.[21–23] We provide an explanation in terms of oxygen diffusion and reduction-oxidation (redox) reactions taking place near the HZO/SrTiO$_{3-\delta}$ interface (Figure 3d–f). As already stated in the introduction, the SrTiO$_{3-\delta}$ film is deliberately grown oxygen deficient since oxygen vacancies act as electron donors for n-type doping.[10] This creates a large O density gradient across the HZO/SrTiO$_{3-\delta}$ heterostructure, which favors diffusion of O^{2-} ions from the HZO interface into oxygen deficient SrTiO$_{3-\delta}$ to establish thermodynamic equilibrium. This tendency is promoted by the surface build-in electric field E_s associated to a finite surface potential Ψ_s. The latter is a combination of the work function difference between the top and bottom (SrTiO$_{3-\delta}$) electrodes and of the negative polarization bound charges, which are accumulated at the lower interface of HZO when it is polarized P_{UP} to write the HRS.

The O^{2-} acceptor diffusion near the interface within $t = t_1 \sim 100$ s compensates the vacancy donors V$_O^{2+}$ and converts SrTiO$_{3-\delta}$ near the interface to an intrinsic semiconductor SrTiO$_3$ (insulating) raising the conduction band minimum away from E_F. As a consequence, the width of the surface potential increases, reducing the free electron density n_e and the current flow through HZO, as depicted in Figure 3e. At longer times, eventually the entire thin SrTiO$_{3-\delta}$ layer will become fully oxidized, intrinsic SrTiO$_3$, and the flow of electrons will become minimal due to small n_e (Figure 3f) as the system relaxes in the energetically most favorable thermodynamic equilibrium
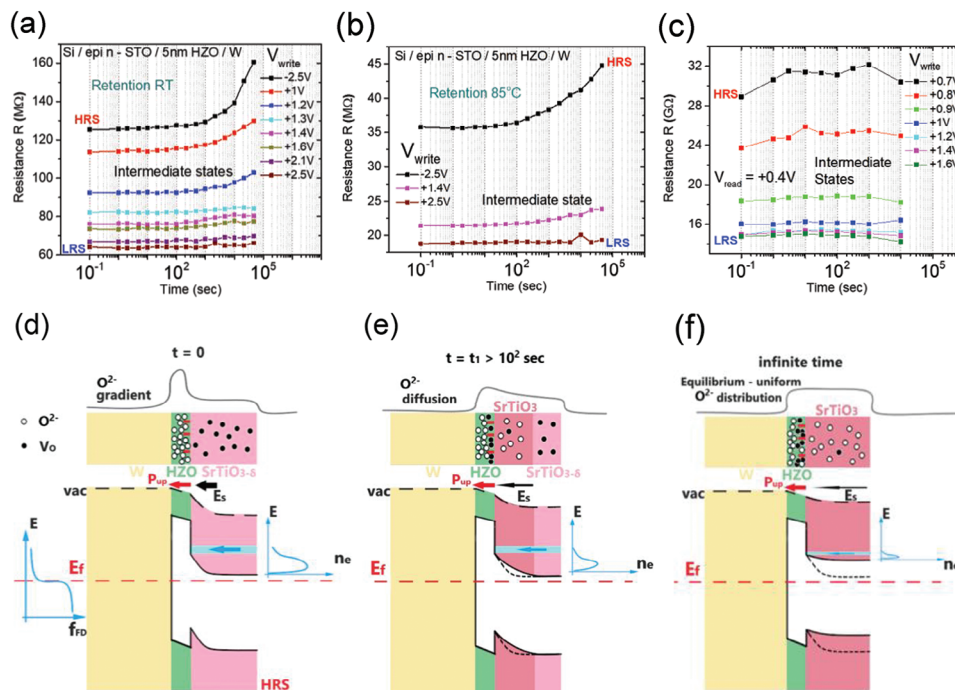
Figure 3. Retention measurements and ionic effects. Retention measurements of a memristive device W/HZO/n-doped SrTiO$_{3-\delta}$ on silicon measured a) at room temperature and b) at 85 °C. c) Room temperature retention of a memristor with bulk Nb:SrTiO$_3$ as the bottom electrode. Schematic illustration of band profile of HZO on oxygen-deficient epi-SrTiO$_{3-\delta}$ for t = 0 d), t ~100 s e) and infinitely long time (f).

situation with nearly flat energy bands, neutral interfaces, negligibly small build-in electric fields and nearly uniform O density across the HZO/ SrTiO$_3$ heterostructure. The interpretation of the HRS drift to higher resistance in terms of oxygen diffusion and redox reactions is further supported by the observations (Figure 3b) that the drift of the LRS and intermediate states becomes larger at 85 °C since at higher temperatures the oxygen movement is facilitated.

The significant role of oxygen movement and redox processes in the HZO / epi n SrTiO$_{3-\delta}$ / Si system is confirmed by the totally different behavior observed on bulk Nb:SrTiO$_3$ (Figure 3c) where Nb doping is used. Since oxygen vacancies are absent in Nb:SrTiO$_3$, there is no oxygen gradient across the HZO/ Nb:SrTiO$_3$ heterostructure and therefore oxygen diffusion and redox processes do not take place in this case. Consequently, the HRS (and all other states) of HZO/ Nb:SrTiO$_3$ devices are constant in time without retention loss (Figure 3c). In the LRS state biased at P_{DOWN}, the uncompensated positive polarization charges at the interface favor low Ψ_s with negligibly small build-in electric field E_s (Figure S8, Supporting Information). In such a case, there is no driving force for O^{2-} ion movement into SrTiO$_{3-\delta}$, especially since the positively charged oxygen vacancies left behind at the HZO near the interface would build more positive interface charges, which is energetically unfavorable. Since there is no oxygen diffusion and redox mechanisms taking place, LRS biased at P_{DOWN} remains stable over time showing excellent retention even at 85 °C (Figures 3b,c).

As discussed above, the ionic motion shows a clear fingerprint in retention measurements. The next step is to find out its impact on the observed resistive loops in Figure 2d. For this purpose, we conducted test experiments with the same device layer structure but without the crystallization annealing, which resulted in amorphous non-ferroelectric HZO. The P-V and the conductance versus voltage curves presented in Figure S9, Supporting Information show no resistive hysteretic behavior. Hence, a potential contribution of SrTiO$_{3-\delta}$ to the resistive switching is excluded. The strong nonlinearity in the resistance-voltage hysteresis loops of Figure 2d is attributed to the effect of ferroelectric switching.

2.4. Time Response of the Devices

The time (or frequency) response of the conductance memory loops for different pulse widths is presented in **Figure 4** (the corresponding resistance loops are shown in Figure S10, Supporting Information). Two distinct effects can be seen. First, we observe a shift of the loops to higher conductance values when the pulse width is increased. Second, we observe a time to voltage trade-off: a larger voltage amplitude is required to switch from HRS to LRS for shorter pulses resulting in wider loops (compare, e.g. 50 ns and 1 ms pulses). The shift of the loops to higher conductance values can be explained by considering the ionic motion in SrTiO$_{3-\delta}$. Before each loop, the device is poled with a long (250 μs) pulse at −1.5 V bringing the SrTiO$_{3-\delta}$ in the intrinsic insulating state (SrTiO$_3$) by pushing O^{2-} ions away from HZO into SrTiO$_{3-\delta}$. Using increasingly longer positive pulse widths for each loop, SrTiO$_{3-\delta}$ converts more and more to the conductive state due to O^{2-} ions moving from its interface and bulk into HZO, resulting in an increase of the conductance of the recorded loops
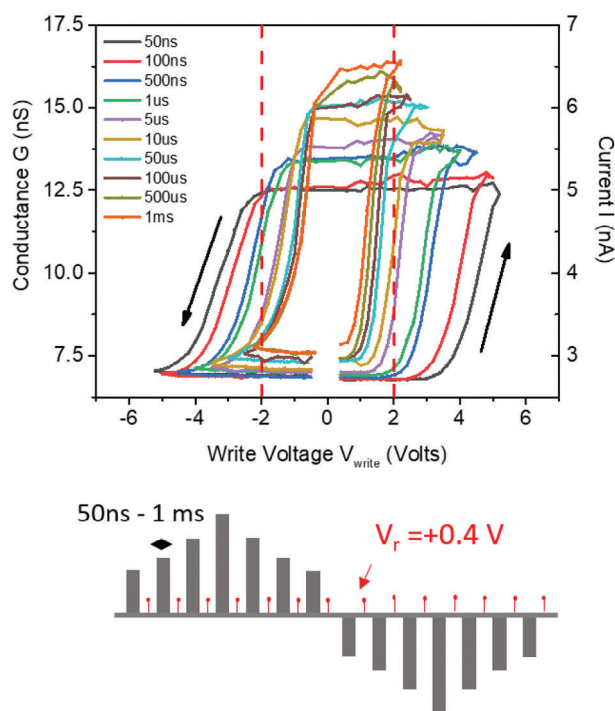
Figure 4. Conductance loops and time-voltage tradeoff in W / HZO / SrTiO$_{3-\delta}$ / Si synapse. Conductance loops as a function of write voltage read for different pulse widths and sketch of the applied pulse scheme. Vr denotes the read voltage. The vertical dashed lines denote the voltage at which the different conductance states can be accessed with pulses of different widths.

and a pronounced increase of the conductance maximum as we move to 1 ms pulses.

The second effect, known as the time-voltage trade-off[14] (the shorter the pulse width, the higher its amplitude in order to switch the polarization, hence, to switch from HRS to LRS) also appears in conventional perovskites (e.g., PZT)[40] but at much shorter pulse widths (sub ns range). In HZO it appears in a wide range of pulse widths, from a few ns to tens of µs.

The time-voltage trade-off behavior is of critical importance for the analog synaptic behavior such as potentiation and depression, in which a number of intermediate states are accessed by using electrical pulse programming. It is apparent from Figure 4 that, in order to exploit the full dynamic range from the lowest to the highest conductance values, it is necessary to set the pulse amplitude to an optimum value of about ±2 V (see red dotted vertical lines in Figure 4). By doing so, we take advantage of the frequency dispersion to access all different states that correspond to the interception points of the two red dotted lines with the different curves in Figure 4.

2.5. Synaptic Plasticity

In **Figure 5**, we show the evolution of the conductance as a function of the number of applied pulses N for different programming schemes. First, we discuss the conductance change when pulses with identical amplitudes (+2 and −2 V) but increasing time width are applied. A large number (more than 13) of inter-

mediate states can be accessed during potentiation and a smaller number during depression leading to an asymmetric line shape (Figure 5a). The symmetry can be significantly improved if the pulse width range is extended down to 50 ns (Figure 5b) suggesting that proper choice of the pulse sequence characteristics is essential to obtain the desired symmetric potentiation/ depression with sufficient number of intermediate states. The potentiation at short timescale, up to 50 µs, is dominated by the frequency dispersion, which reflects the switching dynamics of the ferroelectric HZO itself.

At longer timescales (>50 µs) the increase in conductance with the number of pulses is significantly slowed down (Figure 5a,b), which is attributed to ionic effects in the HZO/SrTiO$_{3-\delta}$ system (see also discussion of Figure 4 above).

From circuit design considerations, driving the synapse with identical pulses is preferable to using variable-width pulses.[12] However, this has been only rarely demonstrated in HZO-based FTJs,[22,23] and indeed with non-ideal, asymmetric potentiation/depression characteristics. Here, we show that in the HZO/SrTiO$_{3-\delta}$ devices, we can access multiple states with identical pulses and near-ideal characteristics. N pulses of 1 µs each were applied sequentially with a short (100 ns) delay time, before the current was read (Figure 5c). This scheme produces time-correlated identical short pulses that allow several intermediate states to become accessible during potentiation. The use of a large number of pulses, e.g. 100, results in asymmetric potentiation/depression since saturation at the maximum value occurs after about 20 pulses. Using only 20 shorter pulses of 500 ns, the potentiation/depression cycle becomes more symmetric and linear (Figure 5d) albeit with a small loss of the dynamic range (smaller difference between maximum and minimum conductance values). More than 16 intermediate states are accessible during potentiation indicating that a multi-state 4-bit memory addressable by identical short pulses is possible in the W/HZO/SrTiO$_{3-\delta}$/Si field-effect memristive device. The observed reduction of the accessible dynamic range after each potentiation/depression cycle is attributed to fatigue due to accumulative effect of a large number of pulses applied between two measurement events.

A comparison of Figure 5a,c shows that the cumulative effect of 10 short and dense pulses of 1 µs each is equivalent to the effect of one pulse of 10 µs. This can be interpreted as follows: during the total duration of a train of N identical pulses of amplitude V, the ferroelectric effectively experiences a single pulse with a width equal to the total duration of the N pulse train with an average bias V' slightly smaller than V (see sketches in Figure 5c,d). When the next pulse trains are applied with larger number of pulses, the effective one pulse width increases so the behavior is similar to that of variable pulse width potentiation and depression. In the limit where the delay time goes to zero, the identical pulse scheme is exactly the same as the variable pulse width one. On the opposite limit, when the delay time between pulses increases, the average bias V' is significantly reduced since the ferroelectric remains at zero bias during longer delay times, therefore, the identical pulses become uncorrelated in time and the dynamic range of the synapse is reduced as shown in **Figure 6**a.

When the delay time becomes sufficiently large (a few seconds) as in the case of isolated identical pulses, the dynamic range is dramatically reduced (Figure 6b, black symbols) compared to
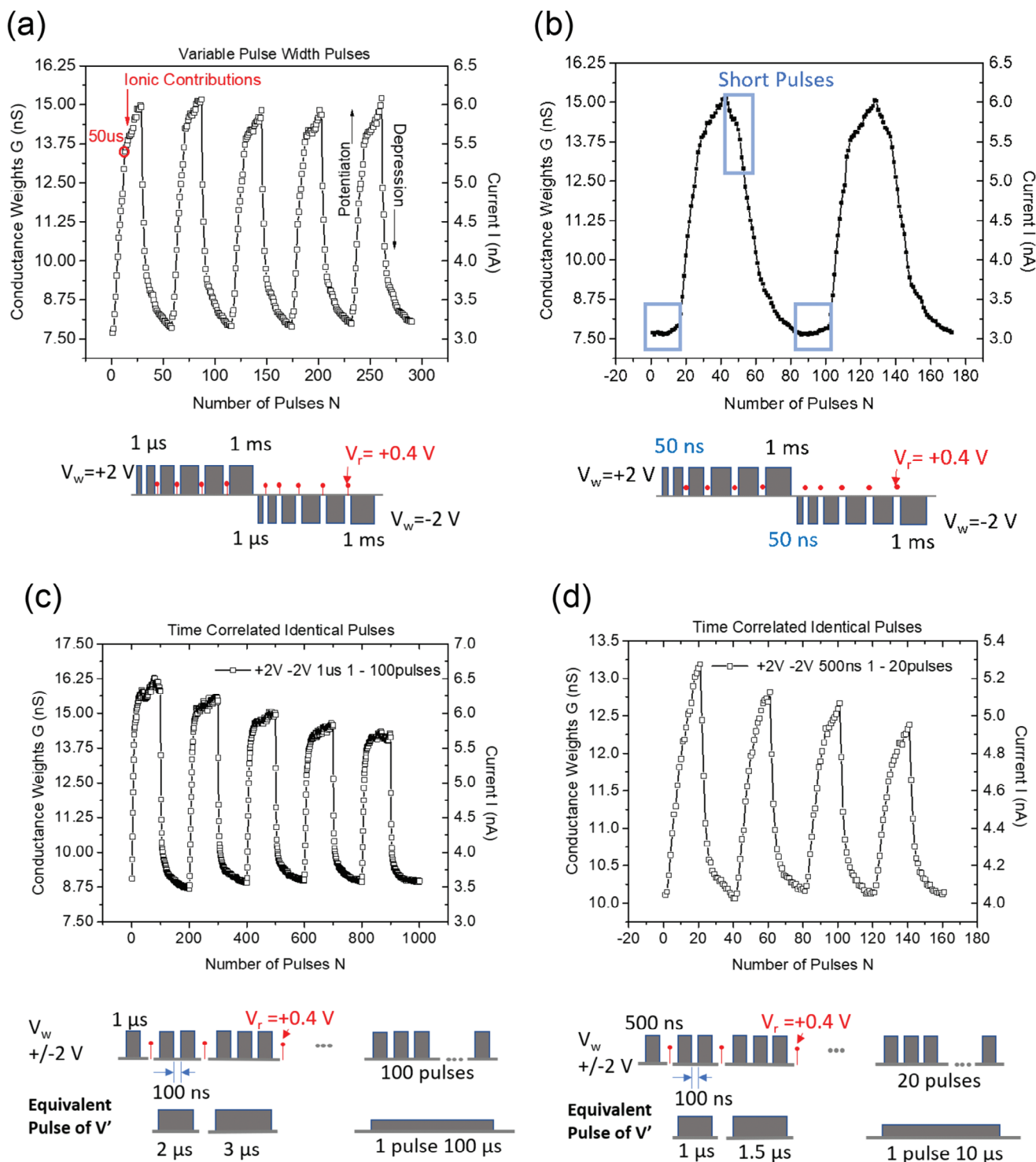
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Figure 5. Potentiation and depression of W/HZO/SrTiO$_{3-\delta}$ /Si synapse for different pulse sequences. Conductance as a function of a) the number of applied pulses for variable width pulses (1 µs – 1 ms), b) the number of applied pulses for variable width pulses (50 ns – 1 ms), c) trains of identical pulses of increasing number (1 – 100 pulses of 1µs, delay 100 ns), and d) trains of identical pulses of increasing number (1 – 20 pulses of 500 ns, delay 100 ns). N is the number of pulses in a pulse train.
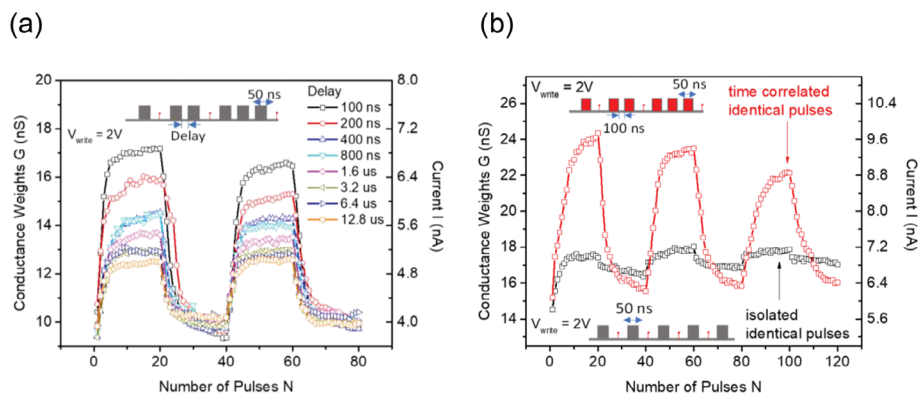
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Figure 6. Effect of delay time on the W / HZO /SrTiO$_{3-\delta}$ /Si synapse dynamic range. a) Conductance weights as a function of the number N of time-correlated pulses in a pulse train with different delay times (100 ns—12.8 µs), b) Potentiation and depression for correlated (red) and uncorrelated (black) identical pulses.

that of identical pulse sequence with a short 100 ns delay (red symbols).

In summary, the delay time between the identical pulses is absolutely crucial for the synaptic behavior. To access a sufficiently large number of intermediate states by identical pulses, the latter must be closely spaced in time. As the delay time between pulses increases, the correlation between them is reduced and the synaptic conductance weights are also reduced.

This can be clearly seen in the pair pulse facilitation (PPF) experiment[41–43] (**Figure 7**), where the changes in conductance weights ΔG were recorded as a function of varying delay time Δt between the two pulses. We observe that the second pulse influences G only at small delay times. The PPF is considered to be a type of short-term plasticity and is used to decode temporal auditory/visual information in biological systems.[41,44]

The HZO/SrTiO$_{3-\delta}$ ferroelectric memristors also show Spike Timing Dependent Plasticity (STDP),[45,8,46] which describes the

strengthening or weakening of the synapses (**Figure 8**) depending on the time synchronization between the pre- and post-neuron firing (spiking) When the time separation Δt is small assuming values near zero, the pulses overlap and their superposition $V = V_{pre}$-V_{post} exceeds the threshold voltage at some instance in time, thus switching the polarization, in which case weakening or strengthening of the synaptic weights are observed as shown in Figure 8. The effect is observed for three different pulse widths (time scales) indicating that STDP can be clearly observed not only in the biological regime of ~ ms but also in much shorter time scales of ≈10–100 ns without significant loss of dynamic range (ΔG max values are all ~ 2 nS) albeit with a penalty of slightly increased voltage as a direct consequence of the time-voltage tradeoff (increase of V_{th} at shorter timescales) as discussed above.

3. Discussion

In this work, we propose a new ferroelectric field effect memristive device, comprising 5 nm ferroelectric HZO epitaxially grown on a 10 or 20 nm SrTiO$_{3-\delta}$ bottom electrode on Si(001). The n-type SrTiO$_{3-\delta}$ semiconductor is more than just an electrode. It adds a critically important functionality to the device. Indeed, the SrTiO$_{3-\delta}$ carrier concentration, hence its resistance, is modulated by the polarization charges via a non-volatile field effect, which depends on the external applied voltage V. Then, the pulse programming can tune the SrTiO$_{3-\delta}$ carrier concentration, hence the total resistance of the device through a number of stable non-volatile states.

Although there is a number of single-layer hafnia-based junctions showing electroresistance typically larger than 4 and in few cases > 1000, there is a rather limited number among them that show synaptic behavior,[19,27,35,46,47,48] mainly potentiation/depression, while fewer show[35,46,47] biological-type of synaptic activity such as STDP. Very few also show potentiation and depression which are obtained with the preferred identical pulse scheme,[19,46,47] the characteristics of which are non-ideal showing asymmetry and non-linearity. In most of the cases,[19,35,46,47] the operation voltage, that is the pulse amplitude used to operate the synapse, is higher than 3 V[19,46] and reaches up to 7 V for thick (10 nm) HZO devices.[35] Remarkably,
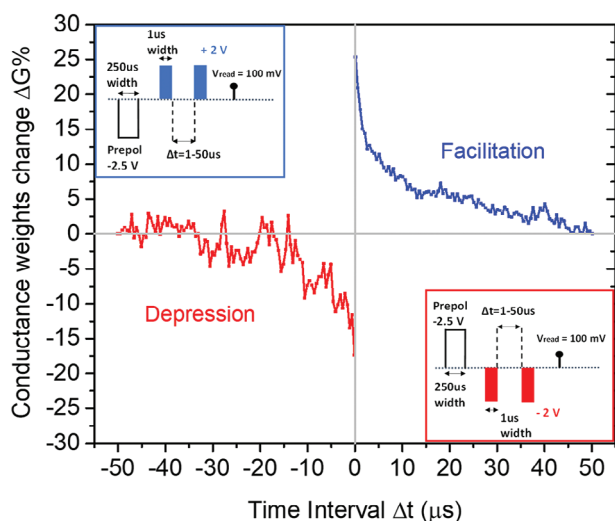

Figure 7. Pair Pulse Facilitation and Depression of the W/HZO / SrTiO$_{3-\delta}$ /Si synapse. Conductance weight change as a result of the application of a second pulse, plotted as a function of delay time Δt between the two pulses.
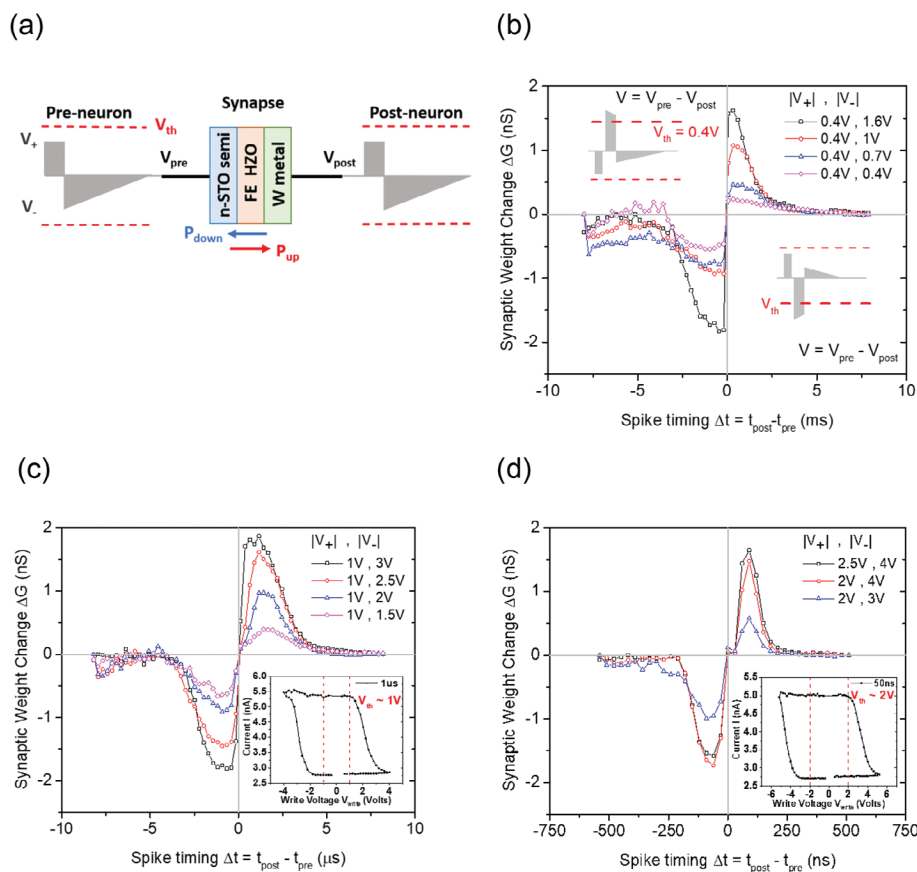
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Figure 8. Spike Time Dependent Synaptic Plasticity of the W / HZO / SrTiO$_{3-\delta}$ /Si synapse. a) Schematic of pre-neuron and post-neuron pulses applied to the HZO / SrTiO$_{3-\delta}$ synapse. b), c), d) Synaptic weight change as a function of the time interval Δt between the pre and post-synaptic pulses for pulses of different duration in the ms, μs, and 100 ns time scale, respectively. The insets in (b) show the combined pulse exceeding the threshold voltage V_{th}. The insets in (c) and (d) show the conductance loops and the corresponding V_{th} values.

a couple of the thinnest HZO junctions of 4.5[48] and 3.5 nm[27] show low operation voltage < 2 V and are comparable to the low voltage results obtained in the present work, but no biological synaptic behavior such as STDP has been reported. Remarkably, STDP in the 500 ns range was reported[46] using low voltage pulses of 2 V which is comparable to that obtained in our work (Figure 8d). However, all types of synaptic behavior in this work[46] were recorded by probing the remanent polarization P_r rather than the current or the resistance which makes this type of devices different than the memristive devices investigated in the present work.

Most of the thick HZO devices of 9[46] and 10 nm[35] are out of the direct tunneling regime and the observed electroresistance is due to other conduction mechanisms as for example thermionic emission over the HZO barrier[35] that requires biasing the device at large voltages (e.g., >5 V in ref[35]). In all other cases where the HZO is sufficiently thin (<5 nm), the authors consider that the electroresistance originates from the modulation of the HZO barrier height and consequently the modulation of the direct tunneling. So all these devices[34–37,47,48] can be classified as FTJs, except for the case of ref[27] where polarization screening by mobile charges in the ferroelectric is considered as the main mechanism of electroresistance. It is worth mentioning that all devices discussed above[19,27,47,48] and the introduction[34–37] with or with-

out synaptic behavior have metallic electrodes and often the bottom electrode is a metallic oxide electrode, mainly LSMO[34–37] but also RuO$_2$[49] or WO$_x$.[27]

To the best of our knowledge, our work is the only one using SrTiO$_{3-\delta}$ as a semiconductor bottom electrode and fully uses the semiconductor properties to obtain finite electroresistance and synaptic behavior in HZO-based junctions. As explained in the discussion about Figure 2e, the HZO ferroelectric induces a non-volatile field effect on the resistance of the semiconductor surface (depletion or accumulation) at the interface with HZO, thus changing the total junction resistance. The semiconductor resistance modulation by the applied voltage (field) plays a pivotal role in electroresistance and it is distinctly different from any other ferroelectric hafnia-based device reported so far. Our devices are epitaxially grown on Silicon which is important for integration and behave as memristors with a number of non-volatile intermediate states. They also show synaptic behavior with nearly ideal symmetric and linear potentiation/depression characteristics obtained with the preferred identical pulse scheme with less than 2 V pulse amplitude, one of the lowest reported in the literature. They also show biological-type synaptic behavior such as PPF and STDP in a wide range of timescales from ms down to 100 ns and with extremely low programming voltage of < 1 V for ms pulses closely matching the biological time response.

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The stability of partial polarization states and therefore of intermediate memristive states is important since it ensures non-volatility. Programming with pulses of variable amplitude or width is normally required to update the conductance weights of stable states, which is not the best programming option. Identical pulses are considered to be the best pulse scheme to drive the synapses since it is compatible with digital circuit design rules without prior knowledge of the initial state. However, the latter scheme is the most difficult to implement since it often results in non-ideal asymmetric and non-linear synaptic characteristics.[20,22,23,48] In this work we show that accessing a large number of intermediate states is possible by time-correlated identical pulses (pulses applied with a short delay of a few hundred of ns between them) using a low programming voltage of around 2 V. This programming scheme takes advantage of the time-voltage trade-off. As already mentioned, this effect is also encountered in conventional perovskite ferroelectrics[40] but only occurs for very short, sub-nanosecond pulses. In the case of HZO, the time-voltage trade-off is more pronounced at larger time scales, from 50 ns to tens of μs, reflecting the fact that switching the polarization dipoles faster requires higher energies (hence higher voltages) than in perovskite ferroelectrics to overcome the rather large ($\approx$1 eV) energy barrier between the two stable polarization states.

Another inherent characteristic property of this new HZO/SrTiO$_{3-\delta}$ electronic synapse is the involvement of ionic (O^{2-}) motion between HZO and SrTiO$_{3-\delta}$ with a clear signature in the retention measurements. The main effect is that the HZO supplies SrTiO$_{3-\delta}$ with O^{2-} acceptors by diffusion to compensate the V_O donors thus converting the thin (10-20 nm) n-doped conductive SrTiO$_{3-\delta}$ to an intrinsic SrTiO$_3$ resistive semiconductor, which affects the resistance of the entire HZO/SrTiO$_{3-\delta}$ device. The drift of the HRS to larger values affects retention in a rather positive way since the memory window increases over time in contrast to what is typically observed in similar devices where the window closes to the point that HRS and LRS cannot be distinguished anymore. Moreover, ionic effects increase the dynamic range of the synapses making more states accessible with longer pulse widths of more than 50 μs, thus increasing the functionality and performance of the ferroelectric synaptic devices. The larger time scale is perfectly compatible with neuromorphic computing applications where signal processing with time scales of 100 ms or larger are involved such as for biological signals.

The large number of stable intermediate states accessible at a low voltage of ±2 V, the possible update of the synaptic weights by identical pulses and the retention properties makes this HZO/SrTiO$_{3-\delta}$ synaptic device particularly attractive for low power analog in-memory computing. The voltage operation can even be reduced to less than 2 V depending on the number of states to be accessed. At 1 V, there are still more than 10 different states that can be accessed. This record low voltage operation is particularly attractive as it is compatible with current CMOS circuits. This is considerably lower than the $\approx$5 V programming voltage in bilayer FTJ stacks, while maintaining a similar current density level.

It is interesting to compare the energy requirements for the programming of a hafnia-based ferroelectric artificial synapse in the STDP mode and in the ms time scale (Figure 8b) with that of biological systems responding in the same timescale. As seen from Figure 8b, the programming pulse can be less than 1 V (the primary, positive square pulse is only 0.4 V) and for such voltage range, the current density is of the order of 10 pA μm^{-2} (Figure 2c). Then, the energy consumed $E_{Joule} = V \times I \times \tau$ due to Joule heating in a scaled 100×100 nm^2 device in a single programming event with $\tau = 1$ ms pulses, would be negligibly small, of $\approx$ 0.1 fJ. In our voltage driven devices, the dominant energy per programming event is the energy $E_{charge} = Q \times V$ consumed to switch the ferroelectric from -P to +P or to charge the capacitor with a charge $Q = 2 \times P \times A$ (P is the polarization, A is the area). Assuming $P \approx 20$ μC cm^{-2}, $A = 100 \times 100$ nm^2 and $V = 2$ V maximum, this energy is estimated to be $\approx$ 8 fJ. This is much smaller than $\approx$10 pJ and $\approx$1 pJ consumed by PCMRAM and OxRAM synapses,[20] respectively, and is comparable to the 10 fJ consumed by biological synapses.[20] Hence, by scaling these devices to smaller areas, extremely low energy consumption in the few fJ range could be possible. With such small energy consumption per programming event, the devices presented here can be used in large and dense cross bar arrays of analog in-memory AI accelerators where power consumption is an issue. The large impedance of the devices could be suitable for minimizing sneak paths and cross talk in these arrays. Nevertheless, the low read current densities ($\approx$ a few pA/μm^2) could be problematic for scaled devices with areas below 100×100 nm since additional sense amplifier circuitry will be needed to read the low currents which are expected to be in the sub pA range. The non-destructive readout and the two-terminal configuration allow better and denser integration in large arrays as compared to FeRAM and FeFET rivals. Finally, since these devices are grown on Si substrates, they can be monolithically integrated with Si circuits in the front end of line but also integrated in the back end of line employing flip chip or wafer bonding routes.[50]

4. Experimental Section

SrTiO$_{3-\delta}$ Epitaxy on Si (001): SrTiO$_{3-\delta}$ films of two different thicknesses (10 and 20 nm) were grown by molecular beam epitaxy (MBE) on p++ and n++ Si substrates. The Si substrates were treated under UV (O$_3$ generator) at 100 °C for 10 min and then loaded into the vacuum chamber. The growth procedure, in situ monitored by reflection high energy electron diffraction (RHEED), involved three main steps.[51] First, the native oxide layer on the Si surface was removed via catalytic desorption of oxygen by depositing metallic Sr and subsequently annealing under ultrahigh vacuum (UHV) conditions at 870 °C until the 2×1 Si surface reconstruction was observed. Additional Sr deposition was then performed followed by UHV annealing at 670 °C to form half a monolayer of Sr with a 2×1 Sr surface reconstruction. Second, Ti and Sr were co-deposited from the effusion cells at a substrate temperature of 380 °C under an O$_2$ partial pressure P(O$_2$) of $\approx 4.5 \times 10^{-8}$ Torr. Third, the films were annealed under UHV at 490 °C to improve the crystallinity. The O$_2$ partial pressure was kept low to deliberately introduce oxygen vacancies in the SrTiO$_{3-\delta}$ layers, as required to serve as a semiconducting bottom electrode.

HZO Deposition on epi-SrTiO$_{3-\delta}$ / Si (100) and HZO Crystallization: HZO (5 nm) was grown by plasma-assisted molecular beam epitaxy (MBE) on SrTiO$_{3-\delta}$/Si in another dedicated UHV chamber by co-evaporating Hf and Zr from e-gun evaporators simultaneously supplying atomic oxygen using a remote RF plasma source.[52] A thickness monitor was used in order to control the evaporation rate of Hf and Zr at the nominal values to obtain the required composition at a ratio Zr/Hf $\approx$1. Atomic oxygen is reactive leading to efficient oxidation of Hf and Zr at low O$_2$ partial pressure of $\approx 1 \times 10^{-5}$ Torr and low substrate temperature of 120 °C to

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produce HZO in the amorphous state. The layers were subjected to crystallization annealing, using rapid thermal annealing (RTA) at 420 °C for 400 s in order to obtain the orthorhombic ferroelectric phase.

For the reference non-ferroelectric HZO, an amorphous HZO (5 nm) film was grown at 120 °C using the same MBE process on $SrTiO_{3-\delta}$/Si substrate. The sample did not undergo any annealing in order to remain in the amorphous state exhibiting dielectric response with no ferroelectricity.

For the reference bulk samples, we used commercially available Nb-doped $SrTiO_3$ (Nb 0.7 at. %) single crystalline substrates. HZO (5 nm) was grown by MBE and annealed by RTA in the same conditions as those described above.

X-Ray Photoelectron Spectroscopy: X-ray photoelectron spectroscopy (XPS) was used to evaluate the n-type characteristic of the epi-$SrTiO_{3-\delta}$ used as the bottom electrode and to derive its free carrier concentration. Measurements were performed using monochromatic AlK_α source (1486.7 eV) and a Phoibos-150 (SPECS GmbH) hemispherical electron analyzer. High-resolution Ti 2p spectrum was recorded using a pass energy of 20 eV, giving an overall experimental energy resolution of 0.3 eV. The take-off angle relative to the sample surface was fixed at 90°, giving a probing depth of $\approx$ 6 nm defined by $\approx 3\lambda$, with λ representing the inelastic mean free path of the Ti 2p photo-excited electron in $SrTiO_{3-\delta}$ while leaving the sample.[53] The deconvolution of the Ti 2p spectrum was performed using CasaXPS software[54]: Shirley background was used to substract the inelastic secondary electron contribution while the elastic Ti peak was modeled using a symmetric Voigt function, a convolution of Lorentzian (30%) and Gaussian (70%).

The XPS data are presented in detail in the Supplementary Information. From the Ti bound state, the oxygen vacancies were estimated to be 0.56 at. % and the corresponding electron density 5.3 - 5.7 $\times 10^{20}$ cm^{-3}.

Spectroscopic Ellipsometry: The optical band gap of the $SrTiO_{3-\delta}$ films was determined from spectroscopic ellipsometry using a Woollam M-2000 system with a wavelength range of 192–1690 nm corresponding to an energy range of 0.73-6.46 eV. The optical index and extinction coefficient (from which the gap was determined) were determined from a Tauc–Lorentz model.[55]

From XPS, E_F is located at 2.7 eV from the valence band maximum, consequently 0.8 eV from the conduction band minimum, given that from ellipsometry, the $SrTiO_{3-\delta}$ film energy gap E_g is estimated to be 3.5 eV.

X-Ray Diffraction, X-Ray Reflectrometry: X-ray diffraction was performed on the $SrTiO_{3-\delta}$ films grown on Si using a Panalytical diffractometer employing Cu K_α radiation. X-ray diffraction measurements on the whole stacks were performed with a Rigaku 9 kW SmartLab system using a parabolic Göbel mirror. The X-ray pole figures were measured with an angular acceptance double Bragg angle of $\Delta(2\theta) = 0.5°$ to ensure reliable counting statistics and sufficient angular resolution. Corresponding simulations of the pole figures were carried out with the WinWulff program package.[56] For X-ray specular reflectometry (XRR) an additional asymmetric 2 x Ge 220 channel-cut crystal collimator was employed to select the Cu Kα_1 line ($\lambda = 1.54056$ Å) and to collimate the primary X-ray beam to about 30 arcsec.

Transmission Electron Microscopy: The cross-section specimens for TEM investigations were prepared using a dual beam (scanning electron microscope-focused ion beam, SEM-FIB) system from Tescan (model Lyra 3XMU). TEM observations were performed using a probe-corrected analytical high-resolution JEMARM 200 F electron microscope operated at 200 kV. The crystalline phase in HZO was identified using several TEM techniques, including conventional and high-resolution imaging (TEM/HRTEM), but also Fast Fourier Transform. The HRTEM patterns and atomic structural models were simulated using the multislice technique with the use of Crystal Kit and Mac TempasX software kits. In each case, series of simulated images were generated according to the sample thickness t and the defocus of the objective lens Δf.

Device Fabrication: The tungsten top electrodes were patterned by optical lithography, W metallization by e-beam evaporation and lift-off. Subsequently, the layers were subjected to crystallization annealing as described above using RTA at 420 °C for 400 s to obtain the orthorhombic ferroelectric phase. Square devices with areas of 300 × 300, 100 × 100 and

50 × 50 µm^2 were fabricated. The n- $SrTiO_{3-\delta}$ electrode was contacted via a broken device at the top.

Electrical Measurements: The basic ferroelectric characteristics (polarization, displacement current, PUND) of the samples were measured using an aixAcct Systems TF Analyzer 1000. The memristive characteristics of the devices (resistance memory loops, synaptic plasticity) were measured using a Keysight Technologies B1500A Semiconductor Device Analyzer equipped with an arbitrary wave function generator and Source Measurement Units (SMUs) capable of measuring low currents below 1pA. A four-arm micromanipulator stage with a vacuum chamber was used to probe the devices at room temperature and 85 °C in vacuum.

To determine the resistivity of the 10 nm-thick $SrTiO_{3-\delta}$ film on an intrinsic Si substrate, we performed 4-point probe measurements using an MPI probe station and a Keysight B1500 semiconductor parameter analyzer. The four tungsten probe needles made contact with the $SrTiO_{3-\delta}$ surface in a straight line, with intervals of ca. 540 µm, as illustrated in the inset of Figure S1b, Supporting Information. During the current sweep ranging from 1 to 10 µA between probes 1 and 4, we measured the voltage drop between probes 2 and 3. The resistivity was then calculated based on the applied current and the observed voltage drop. Notably, given that the resistivity of our intrinsic Si was in the range of 5 kΩ.cm – 1 MΩ.cm , the Si substrate had a negligible impact on the resistivity measurements. Two measurements at different locations yielded nearly identical resistivity values.

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

Conflict of Interest

The authors declare no conflict of interest.

Author Contributions

A. Dimoulas and C. Dubourdieu initiated the study and supervised it. N. Siannas was involved in the growth of HZO layers and performed the electrical characterization. P. Tsipas contributed to the growth and device modeling. C. Zacharaki was involved in the device processing and electrical characterization. D-J. Kim performed the growth of the epitaxial $SrTiO_{3-\delta}$ films on Si, the XRD and the spectroscopic ellipsometry measurements and analyses. W. Hamouda performed the XPS measurements and data analysis. C. Istrate and L. Pintilie performed High Resolution Transmission Electron Microscopy. M. Schmidbauer performed the XRR and X-ray pole figure measurements and corresponding data analysis. A. Dimoulas was involved in the electrical characterization, data analysis and paper writing. C. Dubourdieu was involved in the data analyses and paper writing. All co-authors edited the manuscript.

Data Availability Statement

The data that support the findings of this study are available from the corresponding author upon reasonable request.

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