A Transimpedance Amplifier Using a Widely Tunable PVT-Independent Pseudo-Resistor for High-Performance Current Sensing Applications

Denis Djekic[1], Georg Fantner[2], Jan Behrends[3], Klaus Lips[4], Maurits Ortmanns[1], Jens Anders[1]
Email: denis.djekic@uni-ulm.de
[1]Institute of Microelectronics, University of Ulm, D-89081 Ulm, Germany
[2]Laboratory for Bio- and Nano-Instrumentation, EPFL Lausanne, CH-1015 Lausanne, Switzerland
[3]Department of Physics, Free University of Berlin, D-14195 Berlin, Germany
[4]Berlin Joint EPR Lab, Helmholtz-Zentrum Berlin for Materials and Energy, D-14109 Berlin

***Abstract*— In this paper, we present a pseudo-resistor-based transimpedance amplifier (TIA) whose transimpedance value is PVT-independent and continuously tuneable over a wide range. The nonlinearity of the pseudo-resistors is mitigated by connecting a large number of elements in series and the effect of process variations on the pseudo-resistor is canceled by a biasing network based on a pseudo current mirror. The design is also first order temperature compensated exploiting the PTAT behavior of the proposed pseudo-resistor and using a PTAT current reference for its biasing. The proposed architecture is verified using a prototype manufactured in a $0.18\,\mu\mathrm{m}$ CMOS SOI technology. In this prototype, the transimpedance can be adjusted between approximately $1\,\mathrm{M\Omega}$ and $1\,\mathrm{G\Omega}$. The achievable bandwidth varies inversely proportional with the transimpedance value from around $7\,\mathrm{kHz}$ for a value of $1\,\mathrm{G\Omega}$ up to an opamp-limited maximum of $2\,\mathrm{MHz}$. In the white region, the input referred noise is equal to that of a TIA using an equivalent ohmic resistor. A minimum value of $5\,\mathrm{fA}/\sqrt{\mathrm{Hz}}$ is achieved for a transimpedance of $1\,\mathrm{G\Omega}$. Over a temperature range from $-40\,^{\circ}\mathrm{C}$ to $125\,^{\circ}\mathrm{C}$, the transimpedance varies less than $10\,\%$ for $1\,\mathrm{M\Omega}$. The TIA occupies a chip area of $0.07\,\mathrm{mm}^2$. At room temperature, the power consumption is $9.5\,\mathrm{mW}$ from a single $1.8\,\mathrm{V}$ supply of which the pseudo-resistor consumes $0.2\,\mathrm{mW}$.**

I. Introduction

With the advent of advanced cleanroom manufacturing techniques, which allow for an aggressive sensor miniaturization with significantly reduced intrinsic sensor parasitics, there is a continuous strive for ever increasing temporal resolutions across a large range of disciplines from advanced material science to life science applications. Naturally, this research trend requires the design of improved high-speed readout electronics which preserve the intrinsic sensor bandwidth. Here, current based sensing becomes particularly attractive due to the relatively low impedance levels, which mitigates the effect of residual parasitic capacitances. Therefore, many emerging sensing applications use current-mode sensors to further improve the temporal resolution. This includes e. g. nanopore sensing [1], scanning ion-conductance microscopy (SICM) [2], and electrically detected magnetic resonance (EDMR) [3], to name just a few of them. While there are many possibilities to read out a current signal, opamp-based transimpedance amplifiers (TIAs), cf. Fig 1, provide the best trade-off between noise, linearity, and bandwidth for typical biomedical and material science specifications.

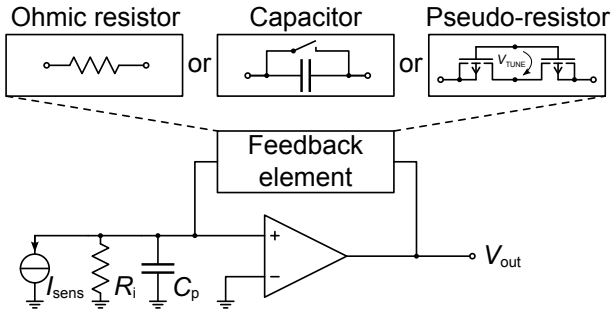

Fig. 1. Illustration of an opamp-based TIA with different possibilities to realize the feedback element.

To realize an opamp-based closed-loop TIA, in addition to the classical resistive TIA, capacitive feedback topologies can be used, cf. Fig. 1, which can improve the trade-off between gain, bandwidth, and the achievable input referred noise. As an example, Ferrari et al. presented an integrator-differentiator TIA with capacitive feedback and additional DC feedback in the first stage [6]. Capacitive TIAs promise improved noise performance due to the absence of the noisy feedback resistor. However, periodic resetting or DC feedback is required to prevent the output from saturation, which leads to a loss of the low-frequency content of the signal or introduces additional noise. Using conventional MOS-diodes in weak inversion as high-value pseudo-resistors, the additional noise is small if no DC current flows through the devices. However, in applications with a nonzero DC current, the noise of the MOS-diodes will exceed that of an equally sized ohmic resistor when the current-dependent shot noise starts to dominate. Moreover, for closed-loop TIAs utilizing DC feedback to cancel the DC part of the input signal, an additional DC signal output has to be provided if DC is a required part of the sensing signal. This, in turn, leads to an increase of area, power, and complexity in calibration and signal processing. Therefore, the resistive feedback TIA topology is still a very attractive candidate for low-power high-performance sensing and there is strong interest to overcome its existing limitations. To achieve this, in this paper, we propose the use of a multi-element pseudo-resistor in the feedback path of an opamp-based TIA, cf. Fig. 2. The proposed circuit is based on the design presented by our group in [5] but significantly extends it to further improve performance and render it immune against PVT variations.

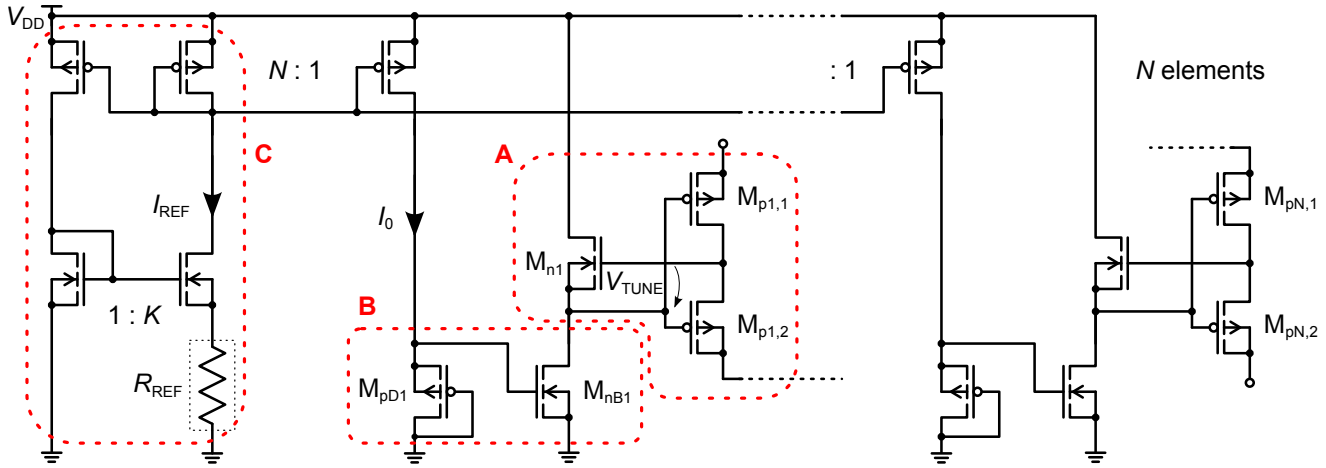

Fig. 2. Schematic of the implemented multi-element pseudo-resistor. A: the pseudo-resistor (p.-r.) proposed by Tajalli in [4]. B: the pseudo current mirror proposed by our group in [5]. A and B form a single p.-r. element. C: the proposed PTAT current reference which compensates the PTAT behavior of the p.-r.

II. Multi-Element Pseudo-Resistor

In [5], we presented a tunable multi-element pseudo-resistor network based on the circuit proposed by Tajalli et al. in [4]. In the original architecture proposed by Tajalli, two PMOS transistors, $\mathrm{M_{p1,1}}$ and $\mathrm{M_{p1,2}}$, are connected back-to-back to form a single symmetrical pseudo-resistor element, cf. Fig. 2A. Its resistance can be tuned via the bias voltage V_{TUNE} whose value is defined by the gate-source voltage of NMOS transistor $\mathrm{M_{n1}}$. Unfortunately, this circuit is very sensitive to PVT variations because the transistors operate in weak inversion and its functionality relies on the matching between PMOS and NMOS devices. To address the problem of process variations, in [5], we introduced a biasing scheme based on a pseudo current mirror whose devices also operate in weak inversion. In this way, the effect of process variations of the devices in the pseudo-resistor are canceled by a reciprocal process dependence in the bias current. The pseudo current mirror consists of the NMOS current source $\mathrm{M_{nB1}}$ which is biased by the PMOS-diode $\mathrm{M_{pD1}}$, cf. Fig. 2B. This results in the desired reciprocal dependence of the bias current on process variations compared to the pseudo-resistor element, in which the PMOS devices are biased by an NMOS device. Thereby, the effect of process variations is canceled and the residual fluctuations in the resistance of the pseudo-resistor element are solely dependent on matching of alike devices, i. e. NMOS with NMOS and PMOS with PMOS.

A second improvement, which was introduced in [5] compared to the original Tajalli architecture, is the series connection of a large number of pseudo-resistor elements. In this configuration, the effect of device mismatch reduces with an increasing number of series elements due to averaging over a larger number of elements while keeping the overall resistance fixed. Moreover, when increasing the number of elements while preserving the total resistance, the voltage drop over a single element decreases and thereby linearity is improved. Finally, connecting many devices in series can also improve the noise performance if the drain-source voltages become sufficiently small for the devices to enter the linear mode of operation where the noise of the pseudo-resistor equals that of an equivalent ohmic resistor. This is an important advantage compared to conventional MOS-diodes in weak inversion, which benefit from the very large resistance around zero drain-source voltage but greatly suffer from shot noise once the drain-source voltage becomes sufficiently large to saturate the device. In contrast, in the presented resistor structure, current-dependent shot noise, which would degrade the noise performance in the conventional structure, does not occur under normal operating conditions since the pseudo-resistor elements always operate in the linear mode. Overall, the connection of multiple elements in series is a crucial improvement regarding linearity, noise, and the effect of device mismatch. However, while connecting a large number of elements in series greatly improves performance, it also introduces stability problems related to the phase shift produced by the RC-ladder network formed by the pseudo-resistors and the well-to-substrate capacitances of the PMOS devices. Here, depending on the utilized technology, the phase shift introduced by the RC-ladder network can severely compromise stability, mandating a relatively large compensation capacitor in parallel to the pseudo-resistor in the feedback path and significantly reducing the achievable bandwidth. To circumvent this problem and allow for the design of high-speed TIAs still using multi-element pseudo-resistors in the feedback path, one can exploit the reduced well capacitance associated with silicon-on-insulator (SOI) technologies. Here, in the case of fully-depleted SOI, these bulk capacitances become close to zero, enabling the design of very high-bandwidth TIAs.

III. Temperature Compensation

In [5], we have shown that the small signal resistance of an N-element pseudo-resistor with pseudo current mirror biasing and ignoring device mismatch is given by:

$$r_{\mathrm{tot}}\Big|_{V_{\mathrm{RES}}=0} \approx \frac{2\mathrm{N}U_{\mathrm{T}}}{I_0}, \tag{1}$$

where $U_{\mathrm{T}} = kT/q$ is the thermodynamic voltage and I_0 is the bias current of the pseudo-resistor element. According to Eq. (1), the temperature dependence of the pseudo-resistors is governed by the PTAT behavior of thermodynamic voltage U_{T} and the temperature dependence of bias current I_0. Here, it is important to observe that if the temperature dependence of I_0 is selected to cancel that of U_{T}, i. e. I_0 also has to be

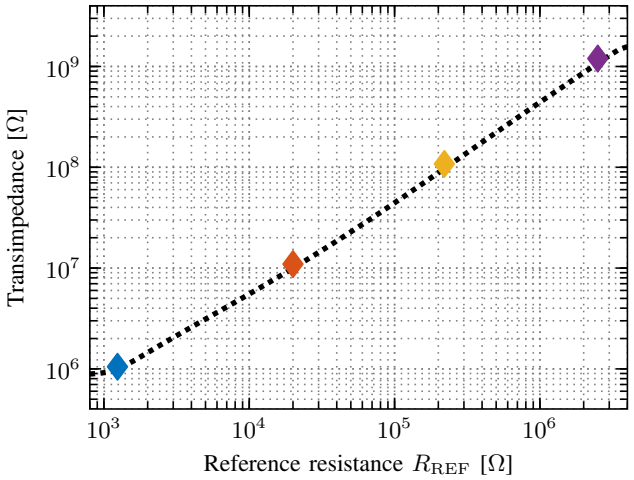

Fig. 3. Transimpedance vs. external reference resistor $\mathrm{R_{REF}}$. The transimpedance can be tuned from 1 MΩ to 1 GΩ. Dotted line: simulated, diamonds: measured

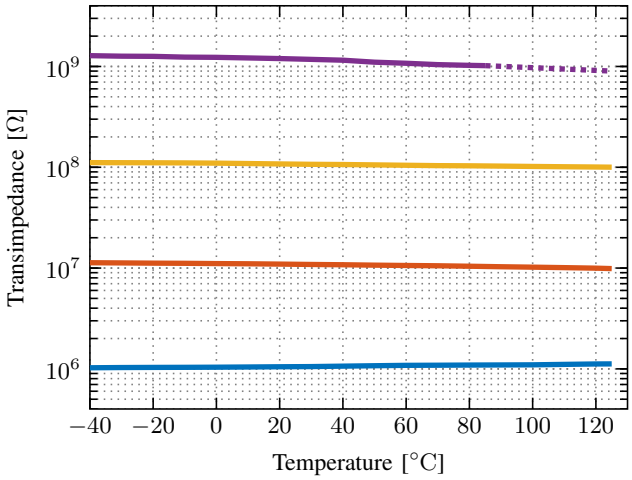

Fig. 4. Measured AC-transimpedances at 100 Hz vs. temperature. The measurement at 1 GΩ was aborted at 85 °C due to the large leakage current of the ESD-protection structure at the input pad

made PTAT, the pseudo-resistor elements become independent of temperature. Fortunately, such a PTAT bias current can be conveniently generated using a beta-multiplier circuit with MOS transistors operated in weak inversion, cf. Fig. 2C, where the generated current I_{REF} is given by:

$$I_{\mathrm{REF}} \approx \frac{n \ln(K) U_{\mathrm{T}}}{R_{\mathrm{REF}}} \tag{2}$$

with slope factor n, reference resistance R_{REF} and multiplier ratio K of the NMOS devices, cf. Fig. 2C. According to Fig. 2, the reference current of the beta multiplier I_{REF} is distributed over all N elements and we therefore have $I_0 = I_{\mathrm{REF}}/N$. Using Eq. (1) and Eq. (2), the total small signal resistance of the cascade of pseudo-resistors can be expressed as a function of the reference resistance R_{REF} according to:

$$r_{\mathrm{tot}}\Big|_{V_{\mathrm{RES}}=0} \approx \frac{2NU_{\mathrm{T}}}{\frac{n \ln(K) U_{\mathrm{T}}}{N R_{\mathrm{REF}}}} = \frac{2N^2}{n \ln(K)} R_{\mathrm{REF}}. \tag{3}$$

As can be seen from Eq. (3), a PTAT reference current according to Eq. (2) indeed leads to a first order cancellation of the temperature dependence of the pseudo-resistors. However, a residual temperature dependence exists due to device mismatch because device mismatch leads to a more complicated temperature dependence of the pseudo-resistor elements than the simple expression of Eq. (1). Hence, a matching aware layout of the pseudo-resistors is crucial to minimize the residual temperature dependence.

IV. Prototype Realization and Measurements

To verify the proposed pseudo-resistor based TIA architecture and temperature compensation scheme, we have implemented a prototype TIA in a 0.18 µm CMOS SOI technology with $N = 16$ pseudo-resistor elements connected in series. The reference resistor R_{REF} has been implemented externally to allow for a convenient tuning of the reference current using a temperature independent resistor. In the presented design, we have implemented a multiplier ratio of $K = 4$, cf. Fig. 2 and Eq. (3). The transimpedance value of the presented TIA can be tuned over a wide range of three decades via the external reference resistance R_{REF}, cf. Fig. 3. The simulated curve (dotted line) exhibits a more pronounced curvature towards small transimpedances where the pseudo-resistors start to enter moderate inversion and deviate from their ideal exponential characteristic. Therefore, the transistion from weak to moderate inversion also defines the lower end of the transimpedance tuning limit. The prototyped TIA provides a minimum transimpedance of approximately 1 MΩ. This value was selected because smaller resistance values can readily be implemented as ohmic resistors using high-resistive layers, which are available in most CMOS technologies. The upper limit of the transimpedance tuning range is determined by leakage currents in the source/drain-bulk junctions. Unfortunately, the number of leakage current sources also increases with the number of cascaded pseudo-resistor elements. Diode leakage currents especially degrade performance at large temperatures because of their exponential temperature dependence. The presented TIA displays an upper limit of transimpedance of approximately 1 GΩ at room temperature. Fig. 4 shows the measured transimpedance vs. temperature behavior for the four discrete transimpedance values highlighted in Fig. 3. The measurement at 1 GΩ was not continued beyond 85 °C because of an excessive leakage current produced by the ESD-protection structure of the input pad. This leakage current was also the reason why all measurements were performed using an AC input signal at 100 Hz. Overall, the measured results of Fig. 4 verify the proposed temperature compensation and the presented TIA shows a small residual variation in transimpedance over the automotive temperature from −40 °C to 125 °C. At 1 MΩ, a variation of less than 10 % is achieved over the entire temperature range with a small residual PTAT behavior, which corresponds to a linear (obtained by a linear regression) temperature coefficient of approximately 600 ppm/K. At 10 MΩ and 100 MΩ, the curves show slight CTAT behavior with a variation in transimpedance over the entire range smaller than 15 % and a linear temperature coefficient of approximately −900 ppm/K. Since the intrinsic temperature dependence of MOS-diodes in weak inversion is exponential, the proposed biasing scheme using a pseudo current mirror in combination with a PTAT reference current greatly reduces the temperature dependence.

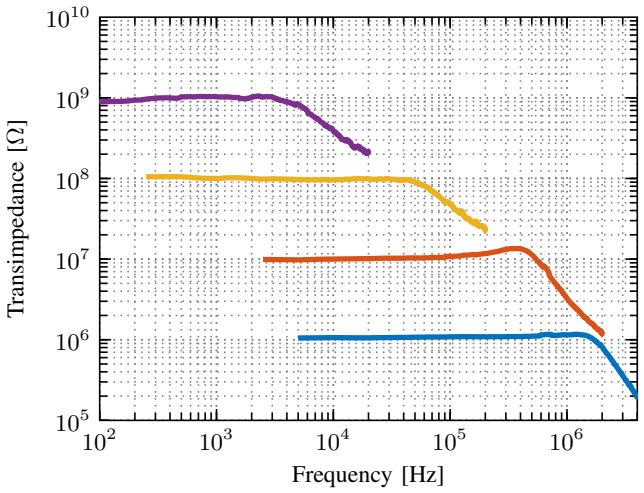

Fig. 5. Measured frequency responses of the presented TIA. For the measurement at 1 MΩ, an additional feedback capacitance of 100 fF has been connected to avoid peaking

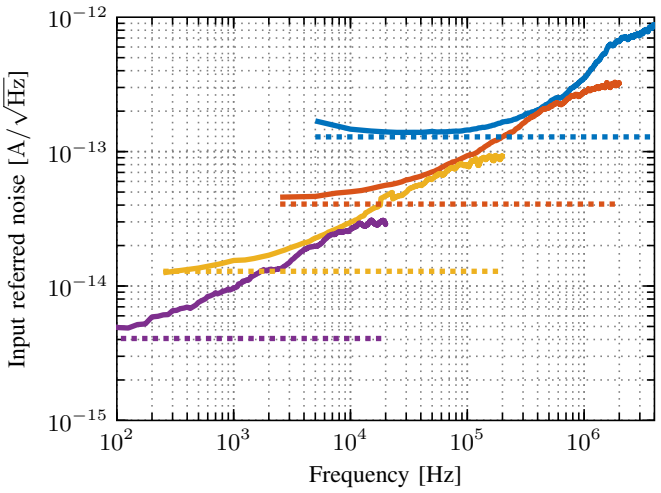

Fig. 6. Solid lines: input referred noise for transimpedances of 1, 10, 100, and 1000 MΩ. Dotted lines: thermal noise of equivalent ohmic resistors.

As explained in Section II, the use of an SOI technology greatly reduces the parasitic well capacitances and thereby minimizes the parasitic phase shift produced by the pseudo-resistor in the feedback path. Nevertheless, the parasitic capacitance C_p at the input of the TIA introduces a second pole in the open-loop gain which needs to be compensated by connecting a small feedback capacitance in parallel to the feedback resistor to ensure stability and avoid peaking. In the presented prototype, a feedback capacitance of $C_\mathrm{fb} = 15\,\mathrm{fF}$ was implemented on chip, which is increased to approximately 22 fF in total because of the parasitic capacitance caused between the test pads on the test PCB.

For frequencies above the flicker noise dominated region, the equivalent input referred noise PSD is given by:

$$S_{\Delta I_\mathrm{n,eq}} = \frac{4kT}{R_\mathrm{tot}} + \omega^2 (C_\mathrm{p} + C_\mathrm{fb})^2 S_{\Delta V_\mathrm{n,OA}}, \qquad (4)$$

where R_tot is the total resistance of the pseudo-resistor, k is the Boltzmann's constant, and $S_{\Delta V_\mathrm{n,OA}}$ is the input referred noise of the opamp. According to Eq. (4), the noise floor is determined by the feedback resistor R_tot and for frequencies beyond the corner frequency of $f = \frac{\sqrt{4kT/R_\mathrm{tot}}}{2\pi(C_\mathrm{p}+C_\mathrm{fb})\sqrt{S_{\Delta V_\mathrm{n,OA}}}}$, the opamp noise starts to dominate, cf. Fig. 6.

V. Conclusion

A new TIA architecture utilizing a PVT-independent multi-element pseudo-resistor as feedback element has been presented together with a prototype realization in 0.18 µm SOI CMOS. The temperature compensation is achieved by biasing the pseudo-resistors using a pseudo current mirror in combination with a PTAT reference current. The manufactured prototype verifies the proposed temperature compensation with a small residual variation of approximately 10 % over the full automotive temperature range. Moreover, the prototype shows a wide transimpedance tuning range of three decades. Thanks to the utilized SOI technology with its reduced parasitics, the achieved bandwidth renders the proposed TIA architecture an excellent candidate for emerging current sensing applications in biomedical and material science research.

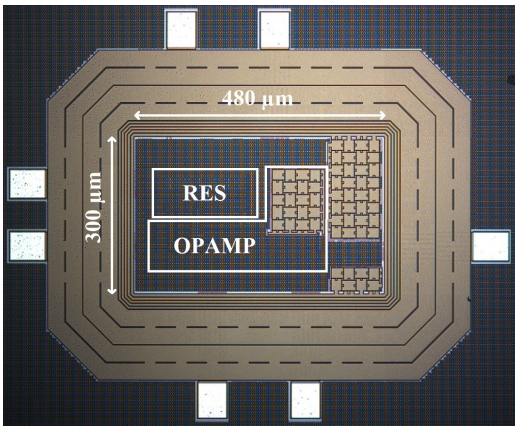

Fig. 7. Die micrograph. The TIA consumes 200 µm x 350 µm of chip area of which the proposed pseudo-resistor consumes only 80 µm x 200 µm including compensation capacitance, blank switch, and dummy structures.

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