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Amorphous GaO_x based charge trap memory device for neuromorphic applications

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ABSTRACT

In this work, we demonstrate a 3-terminal field-effect based charge trap memory device with an amorphous-GaO_x (a-GaO_x) layer fabricated at a low deposition temperature of 250°C. Utilizing the long life-time traps in the a-GaO_x/Al_2O_3 stack, we study the charge trap memory effect in the field effect devices. We observe more than one order of magnitude in channel current difference for two memory states with a retention of more than 10^2 s and endurance of 100 cycles. Our work paves a way for embedded a-GaO_x memories for neuromorphic applications.

1. Introduction

Amorphous oxide semiconductors have been extensively studied for use in thin-film transistor display technology as they offer high conductivity combined with optical transparency. Their conductivity can be tuned through deposition processes and can be better than low temperature (<400°C) deposited amorphous or polycrystalline Si, making them suitable for back-end-of-line (BEOL) integration. Furthermore, metal oxide semiconductors also have several interesting properties, particularly the memristive property, which makes them suitable for memory applications. In this context, amorphous indium gallium zinc oxide (IGZO) and indium zinc oxide (IZO) have gained interest as materials for embedded DRAM and memories for synaptic application through BEOL integration on CMOS technology [1,2]. Amorphous gallium oxide (a-GaO_x) is a transparent conducting oxide with a wide bandgap (~4.9 eV) and can be n-type doped, yet it is much less investigated. The n-type doping in a-GaO_x seems to result from oxygen defects [3,4]. Therefore, a-GaO_x has the advantage of robust carrier density control as it does not require alloying or stable alloy composition, unlike other metal oxide semiconductors such as IGZO. Additionally, the low processing temperature of a-GaO_x by atomic layer deposition enables applications such as BEOL integrated ultra-low power memories or embedded memories, which are intensely being pursued for neuromorphic and in-memory computing [5]. For neuromorphic computing, both volatility and non-volatility in memory devices is of interest, as volatile memories can be used for neuron functions and non-volatile ones for synaptic behaviour [6]. Therefore, devices that can be used as embedded DRAM (volatile) or as charge-trap transistors, memristors (non-volatile) are of great interest. Two terminal memristive devices are popular for BEOL integrated memories; they operate with write currents in the range 10 – 100 μA (10 – 100 kΩ resistance). Three terminal field effect devices have the advantage that they can operate at reduced currents in the nano ampere range (MΩ to GΩ resistance), leveraging the gate control of the current, and are thus useful for low power applications. Metal oxide channel field effect devices can be excellent candidates for ultra-low power BEOL memories for neuromorphic computing as they feature generally low current densities compared to filamentary memristors. In this work, we propose an a-GaO_x channel non-volatile memory device, based on a charge trap mechanism resulting from charge traps near the a-GaO_x channel and bottom oxide interface. We show that the memory effect survives several program and erase cycles, and the states have a retention of more than 100 s. We also show that multiple states can be obtained with repeated application of erase pulses demonstrating potentiation behaviour necessary for neuromorphic applications.

2. Device fabrication

We fabricated a-GaO_x conductive layer-based devices with 22 nm a-GaO_x as the channel layer and 20 nm Al_2O_3 as the bottom insulator on a highly doped p^{++} Si substrate. The a-GaO_x thin film and Al_2O_3 bottom oxide were deposited using plasma-enhanced atomic layer deposition

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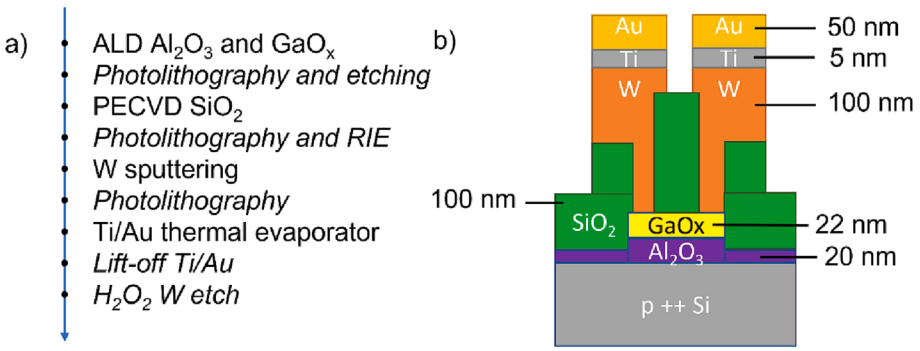

Fig. 1. a) Process flow of the sample fabrication, b) cross-section schematic of the device stack.

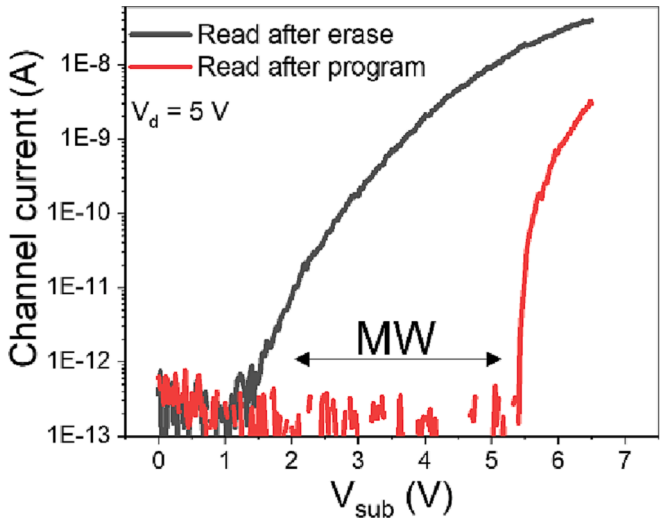

Fig. 2. Read current with field-effect of the a-GaOx layer after program (12 V for 500 ms) and erase (−7 V for 1 s) pulses for a device with 8 μm length and 10 μm channel width, indicating the memory window (MW). The substrate voltage is swept to 6.5 V with V_d = 5 V.

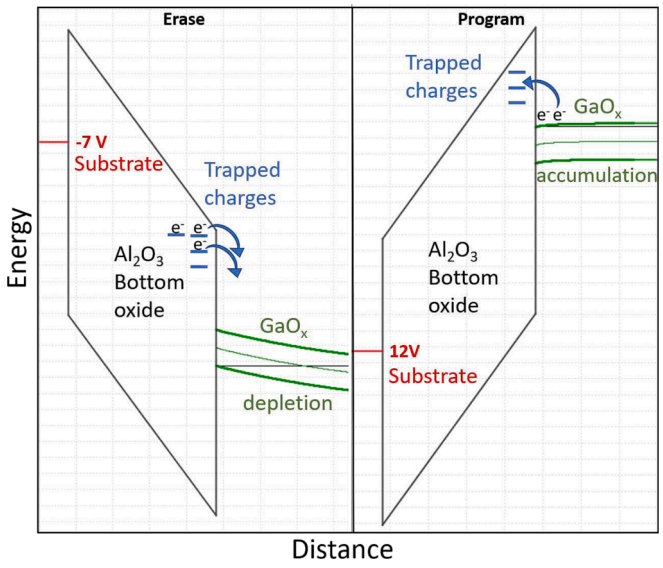

Fig. 3. Schematic band diagram showing the charge-trap mechanism during the erase and program states of the device [16].

(PEALD) at 250 °C. The a-GaO_x PEALD process developed [3] allows tuning of the a-GaO_x layer conductivity through O_2 plasma exposure time during each cycle of the deposition. The bottom oxide and channel were first deposited on a p^{++} Si substrate. The channel mesa was then patterned using photolithography and etched by the resist developer. Afterwards, 100 nm SiO_2 was grown by plasma-enhanced chemical vapor deposition as the encapsulation layer and contacts in the layer were opened using CHF_3-based reactive ion etching. A 100 nm thick W contact layer was then deposited by sputtering and patterned with a Ti (5 nm)/Au (50 nm) as hard mask during wet etching of the W in a 30% H_2O_2 solution. The process flow is shown in Fig. 1a and the schematic of the resulting device in Fig. 1b. Devices with several channel lengths and widths were fabricated on the same chip. In this paper we discuss the results for devices with 10 μm channel width and 8 μm channel length. The electrical characterization of the devices was performed using a Keysight B1500 semiconductor parameter analyser.

3. Results and discussion

The measurements of the current through the a-GaO_x layer were performed by applying a voltage bias on the p^{++} Si substrate (noted V_{sub}) for field effect and a drain voltage (noted V_d) across the channel layer. In order to demonstrate charge trap memory effect, the following measurements were performed. The device was subjected to a 'program' pulse (12 V on the substrate for 500 ms) and an 'erase' pulse (−7 V on the substrate for 1 s). After the program and the erase pulse a 'read' measurement was performed. The read measurement consisted of sweeping the substrate voltage from 0 to 6.5 V with a constant drain voltage of 5 V across the channel. The read current *versus* substrate voltage curves are shown in Fig. 2. A clear change in the channel current is observed between program and erase operations, confirming the memory effect. The mechanism we hypothesize is similar to the one of metal–nitride–oxide–silicon (MNOS) transistors [7]. The band diagram schematics for program and erase operations are shown in Fig. 3. Due to the high field, the gate oxide energy barrier has a trapezoidal shape. This condition is similar to Fowler-Nordheim (FN) tunneling case. However, here the charges only tunnel in and out of the trap states in the oxide to and from the conduction band of the channel layer. This tunnelling from trap states to the conduction band could be considered similar to FN tunnelling. During the erase state the negative voltage bias (−7 V) on the substrate brings the a-GaO_x channel into depletion, allowing the interface traps in the Al_2O_3 bottom oxide layer to de-trap electrons (and probably also inject holes from a-GaO_x layer into deep traps in Al_2O_3) effectively increasing the net positive charge in the bottom oxide. It results in lowering the substrate voltage needed to accumulate carriers in the channel. Hence, one can obtain a high current at a read substrate voltage pulse of 6.5 V. Inversely, during the program operation, the positive voltage bias (12 V) on the substrate brings the a-GaO_x layer into the accumulation region, allowing the electrons from the a-GaO_x conduction band to be injected into the trap states in the Al_2O_3 layer. It effectively increases the net negative charge in the bottom oxide (or

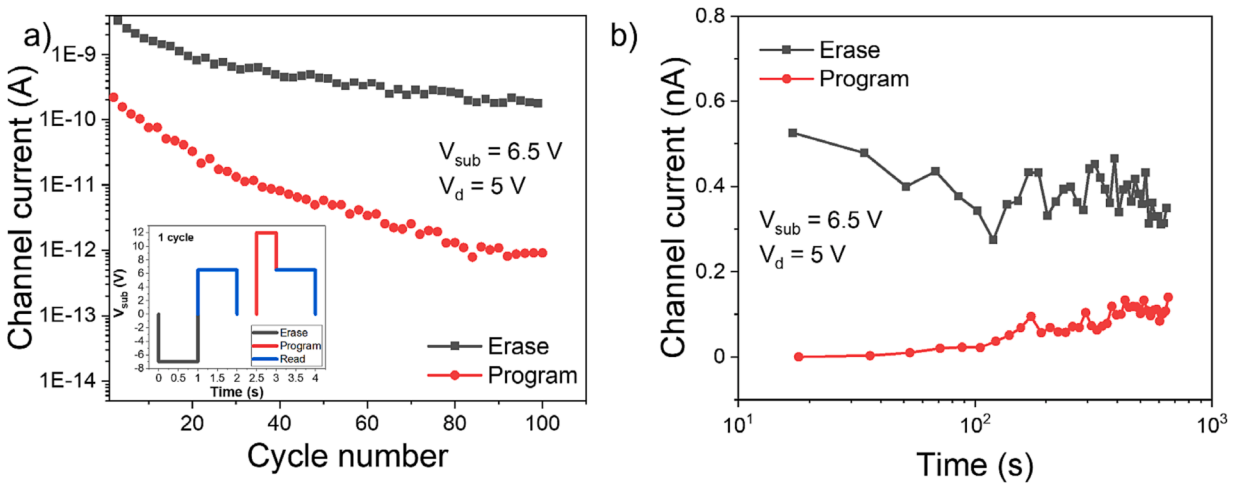

Fig. 4. a) Endurance and b) retention measurements for a device with 8 μm length and 10 μm channel width. The inset graph shows a schematic of the voltage pulses applied during 1 cycle. An erase pulse of −7 V for 1 s is applied, followed by a read pulse of 6.5 V and a program pulse of 12 V for 500 ms followed by the same reading pulse of 6.5 V. This is repeated for 100 cycles.

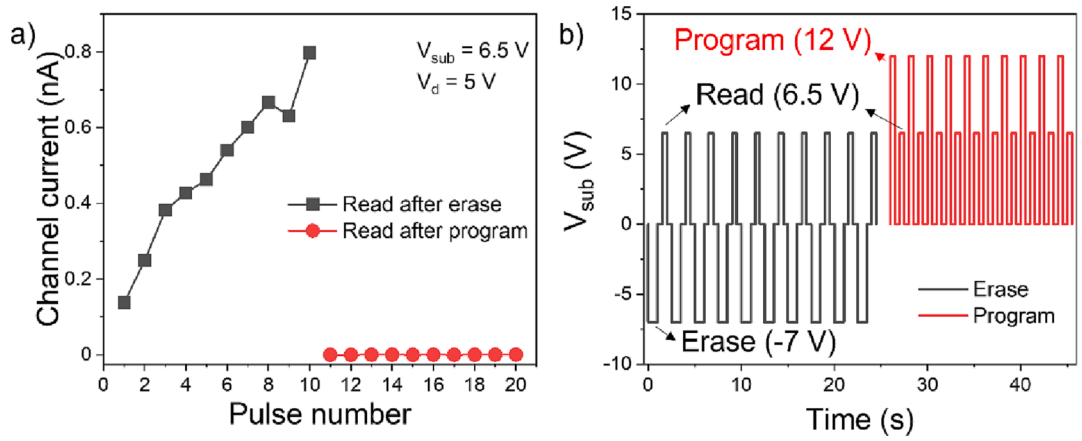

Fig. 5. a) Multiple states measurements showing 10 different states with erase pulses, followed by program pulses. Measurements data for a device with 8 μm channel length and 10 μm channel width. b) Schematic of the pulse voltage applied during the measurements shown in Fig. 5 a. An erase pulse of −7 V is applied for 1 s followed by a read pulse of 6.5 V. This cycle is repeated 10 times. Afterwards a program pulse of 12 V is applied for 500 ms and followed by a read pulse of 6.5 V and repeated 10 times.

lowers the net positive charge). As a result, a higher substrate voltage is needed to accumulate electrons in the channel. Hence, a lower current compared to the one in the erase state (due to low channel charge) is obtained at 6.5 V read substrate voltage pulse. While the conventional MNOS memory device has a tunnelling oxide and a charge trap oxide, here we have only one bottom oxide. Therefore, we believe that the charge traps are near the interface in the Al_2O_3 bottom oxide. Prior studies indicate that there are deep traps in the Al_2O_3-Ga_2O_3 interface, which might be present in our device [8]. While the absence of tunnel oxide could cause low retention, if the traps have long life-time the retention might still be sufficient for low power bio-realistic neuromorphic circuits [9,10] where time scales of several seconds to minutes are sufficient. We performed switching cycles (endurance measurement) for 100 cycles as shown in Fig. 4a. Although there is a drift in the current during the endurance measurements, the memory window is maintained and stabilizes after 80 cycles. Furthermore, the retention measurement on the device shows a clear memory window up to 650 s as shown in Fig. 4b. The memory window is decreased to around 200 pA after 650 s. While low current can be a limitation for classic high speed memory application, a difference of 200 pA can still be identified with sensitive amplifier circuits [11]. A recent work has shown neuron circuits operating with 100 pA range current [12]. The retention was measured after the device had been cycled several times beforehand and therefore starts with a slightly lower current for both programmed and erased state compared to pristine state (1st cycle in endurance measurement; Fig. 4a). While the retention is lower compared to conventional charge-trap flash memory devices (>10^4 s), it is still long enough to be utilized in low power neuromorphic circuits for bio signal processing [10]. Our devices exhibit conductance in the order of 20 nS, which is lower in comparison to similar works on amorphous oxide channel non-volatile devices, showing a range of 100–2000 nS [13–15]. The lower conductance value in our devices has the potential to enable lower power consumption in neuron circuits. Moreover, the ease of integration of these Al_2O_3-a-GaO_x 3-terminal devices on BEOL of neuromorphic chips opens opportunities to develop hybrid neuromorphic circuits utilizing a-GaO_x memory and Si CMOS transistors.

Finally, we investigated the possible presence of multiple memory states in these devices. To do so, we applied 10 consecutive erase pulses of −7 V and 1 s pulse width on the device. These pulses were followed by 10 program pulses of 12 V (500 ms pulse width). The results are presented in Fig. 5. We show that 10 different current states can be reached with repeated application of erase pulses. Thus, the device has potential for use in electronic neuron circuits as it can demonstrate integration of erase pulses and has slow decay of the current state (inferred from lower

retention in Fig. 4b). The program pulse application shows binary nature and leads to abrupt drop in current. These are promising first results on BEOL compatible oxide channel material and can be further optimized through stack engineering and electrical programming optimization.

4. Conclusion

We demonstrated a low temperature (250 °C) ALD-grown conductive a-GaO_x based memory device. Based on the charge traps in the oxide channel - gate oxide stack, programmed and erased current states with a ratio of more than one order of magnitude were obtained. The states also show a retention of more than 10^2 s and are stable over several cycles. By application of several identical erase pulses about 10 distinguishable states are obtained, demonstrating the potential for neuromorphic applications. As this is a novel demonstration of a 3-terminal a-GaO_x based memory device, further engineering of the stack can be done to improve the stability of memory states. Furthermore, adding an extra blocking or tunnelling oxide as in the MNOS devices could improve the retention towards embedded memory applications. Our work demonstrates a novel amorphous oxide material-based device for BEOL-integrated memories for neuromorphic applications.

Declaration of Competing Interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

Data availability

Data will be made available on request.

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